CS4282P

High Performance Stereo Audio Codec

Features

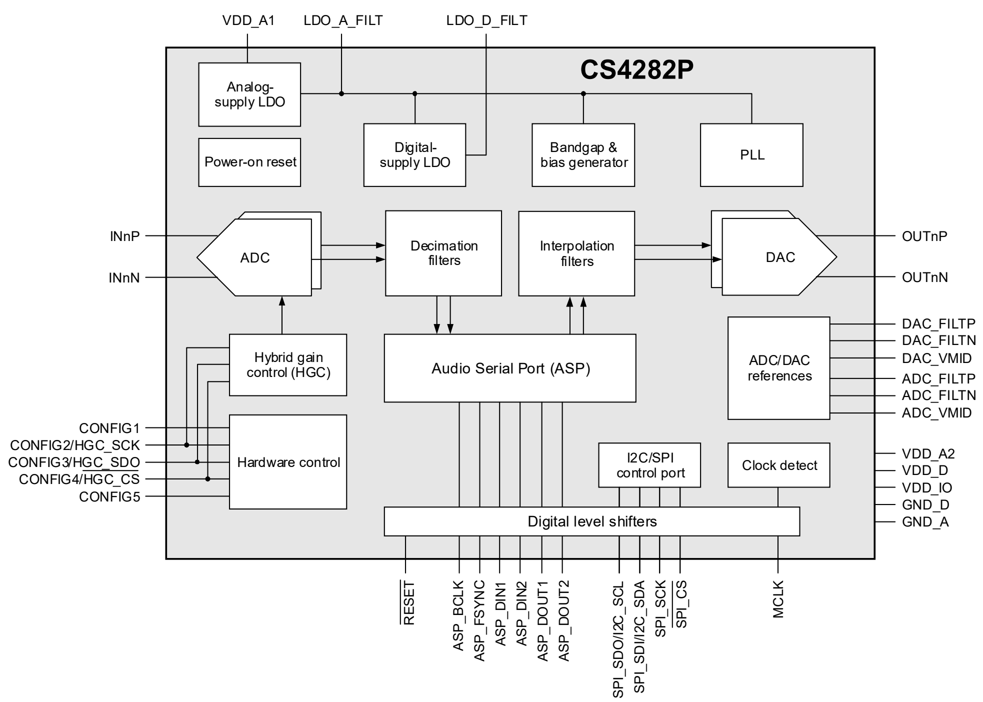
- High performance two-channel codec
  - Differential analog architecture
  - High-resolution 32-bit digital architecture
  - Low-latency digital filters and digital volume control
- Current-mode output for optimal dynamic range into application-specific output buffer
- PLL supports range of external system-clock references
- Sample timing alignment across multiple devices
- Synchronized control of external preamplifier gain
- Audio serial port (ASP) sample rates up to 768 kHz
  - I²S, left-justified, and TDM data formats
- Hardware and software control modes
  - I²C control port up to 1 MHz
  - SPI control port up to 24 MHz
  - Hardware control with no host processor required
- Single-supply operation at 3.3 V
  - Support for 1.8 V–3.3 V digital input/outputs
- 48-pin QFN package

Specifications

- Advanced multibit sigma-delta ADC
  - 123 dB dynamic range (A-weighted)
  - –110 dB total harmonic distortion + noise (THD+N)
  - 4.1/Fs group delay at 96 kHz sample rate (slow roll-off, minimum-phase filter)
  - 2 V_{RMS} differential analog input
  - High-pass filter
- Enhanced oversampling sigma-delta DAC
  - 128 dB dynamic range (A-weighted)
  - –115 dB total harmonic distortion + noise (THD+N)
  - 4.5/Fs group delay at 96 kHz sample rate (slow roll-off, minimum-phase filter)

Applications

- A/V receivers
- Digital mixing consoles
- DAW interfaces
- Musical instruments



Advanced Product Information

This document contains information for a product under development. Cirrus Logic reserves the right to modify this product without notice.

DS1318A3
DEC 2024

General Description

The CS4282P is a high-performance, 32-bit resolution, stereo CODEC. The CS4282P supports differential analog input/output, and 32-bit digital input/output via the audio serial port (ASP) at sample rates up to 768 kHz.

The ADC uses a differential architecture, optimized for high performance combined with low power consumption. The CS4282P uses a 5th-order, multibit sigma-delta modulator followed by digital filtering and decimation.

The DAC incorporates a proprietary analog FIR architecture to reduce out-of-band noise and minimize the external component requirements. Configurable low-latency digital-interpolation filters are provided. The differential current-mode output enables a single-stage external op-amp circuit to combine the current-to-voltage conversion and out-of-band filtering, supporting flexible integration and optimal dynamic range for the target application.

The CS4282P can be configured using a control interface supporting I^{2}C and SPI modes of operation. The device can also be operated in hardware mode, using external resistors to select the required configuration. Multiple hardware-control options are supported, including system clocking, ASP format, sample rate, and digital-filter selection.

The low-latency digital filters are optimized for the applicable sample rate. Fast or slow roll-off filters can be combined with minimum or linear phase responses to support the desired signal characteristics. A de-emphasis filter is also available.

The CS4282P supports synchronized control of an external preamplifier associated with each ADC input path. Updates to the external and internal gain settings are fully synchronized, and a transient-masking function provides additional capability to ensure seamless operation across all signal levels.

The ASP supports multichannel operation in I^{2}S, left-justified, and TDM data formats. Two data-output pins and two data-input pins support 32-bit operation up to 768 kHz. Tristate control of the data-output pins allows multiple devices to operate on a shared bus.

Clocking for the CS4282P can be derived from the ASP, or else provided from a separate clock source. An integrated phase-locked loop (PLL) is used to reduce jitter and to support a range of reference-clock frequency options. The ADC-sample and DAC-conversion timing is referenced to the ASP data frame, enabling time-aligned operation across multiple devices sharing a common data bus.

The CS4282P can be powered from a single 3.3 V supply; an integrated regulator provides the 1.2 V digital-core supply. Digital input/output at 1.8 V logic levels is also possible using a separate external supply. The device combines high performance with low power consumption.

The CS4282P is available in a commercial-grade 0.4 mm pitch, 48-pin QFN package for operation from –40° to +85°C.

See Section 11 for ordering information.

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1 Pin Assignments and Descriptions

1.1 48-Pin QFN (Top View, Through-Package)

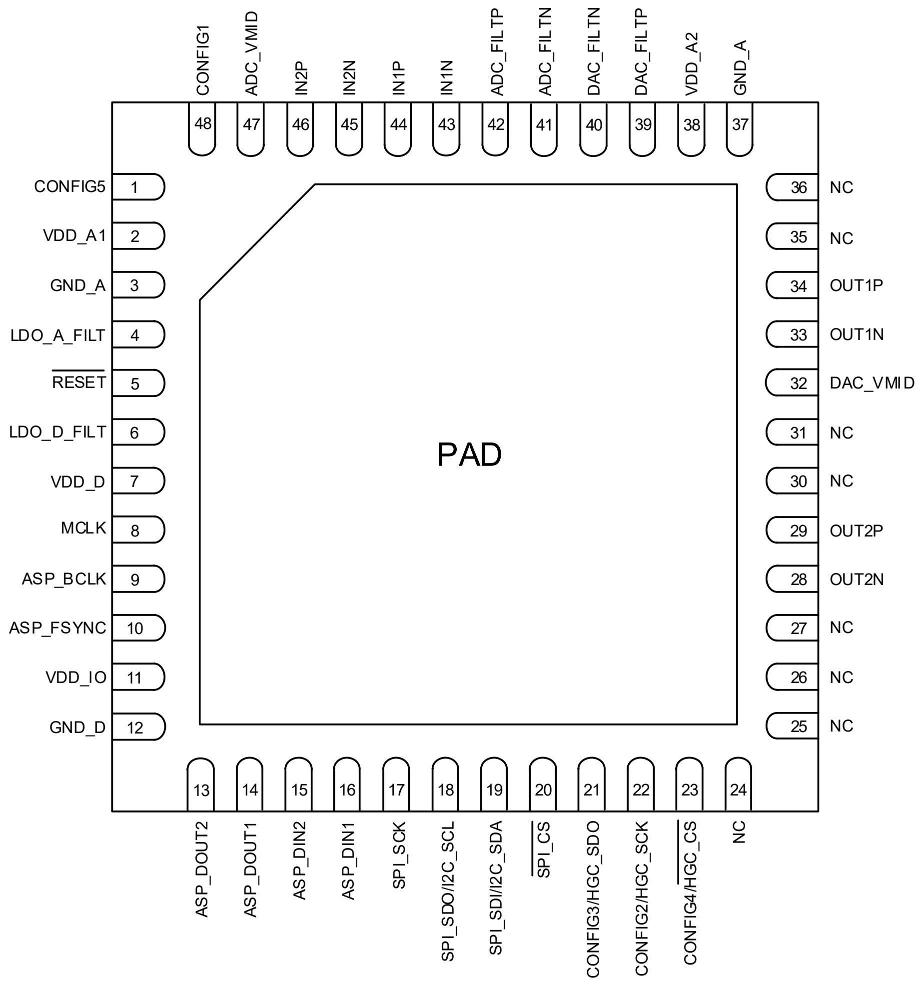


Figure 1-1. QFN 48-pin diagram (Top View, Through Package)

1.2 QFN Pin Descriptions

Table 1-1. QFN Pin Descriptions

Pin Name	Pin #	Power Supply	I/O	Description
				Digital I/O
ASP_BCLK	9	VDD_IO	I/O	Audio serial port bit clock.
ASP_DIN1 ASP_DIN2	16 15	VDD_IO	O	Audio serial port data input.
ASP_DOUT1 ASP_DOUT2	14 13	VDD_IO	O	Audio serial port data output.
ASP_FSYNC	10	VDD_IO	I/O	Audio serial port frame sync.
MCLK	8	VDD_IO	I	Master clock input.
$\overline{\text{RESET}}$	5	VDD_IO	I	Hardware reset control (active low).
$\overline{\text{SPI\_CS}}$	20	VDD_IO	I	SPI chip select (active low).

Table 1-1. QFN Pin Descriptions *(Cont.)*

Pin Name	Pin #	Power Supply	I/O	Description
SPI_SCK	17	VDD_IO	I	SPI clock.
SPI_SDI/I2C_SDA	19	VDD_IO	I/O	SPI data input/I2C data input/output.
SPI_SDO/I2C_SCL	18	VDD_IO	I/O	SPI data output/I2C clock input.
				Analog I/O
ADC_FILTN ADC_FILTP	41 42	VDD_A	O	ADC external capacitor connection. ADC_FILTP should be connected to VDD_A1 via a 1 Ω resistor.
ADC_VMID	47	VDD_A	O	ADC mid-rail voltage reference output.
CONFIG1 CONFIG2/HGC_SCK CONFIG3/HGC_SDO CONFIG4/$\overline{\text{HGC\_CS}}$ CONFIG5	48 22 21 23 1	VDD_A VDD_IO VDD_IO VDD_IO VDD_A	I/O	Hardware control pins. In software control mode, CONFIG2–4 support the hybrid gain control (HGC) SPI controller interface. In software control mode, CONFIG5 selects the I2C target address.
DAC_FILTN DAC_FILTP	40 39	VDD_A	O	DAC external capacitor connection. The DAC_FILTP capacitor should be connected to VDD_A2.
DAC_VMID	32	VDD_A	O	DAC mid-rail voltage reference output.
IN1N IN1P	43 44	VDD_A	I	Analog Input 1.
IN2N IN2P	45 46	VDD_A	I	Analog Input 2.
LDO_A_FILT	4	VDD_A	O	LDO_A regulator external capacitor connection.
LDO_D_FILT	6	VDD_A	O	LDO_D regulator external capacitor connection.
OUT1N OUT1P	33 34	VDD_A	O	Analog Output 1.
OUT2N OUT2P	28 29	VDD_A	O	Analog Output 2.
				Power Supplies
VDD_D	7	—	—	Digital supply (powered from internal LDO)
VDD_A1	2	—	—	Analog supply
VDD_A2	38	—	—	Analog supply
VDD_IO	11	—	—	Digital I/O supply
GND_D	12	—	—	Digital ground [1]
GND_A	3, 37, PAD	—	—	Analog ground [1]
				No Connect
NC	24, 25, 26, 27, 30, 31, 35, 36	—	—	No connect

1.All ground pins, including the ground paddle, must be tied to a common ground plane directly underneath the CS4282P.

1.3 Termination of Unused Pins

Table 1-2 shows the required termination for unused pins (i.e., if the functionality of the pin is not being used). Pins not listed must be connected as shown in the typical connection drawings (see Section 2).

Table 1-2. Termination of Unused Pins

Name	Termination if unused
ASP_DOUTx	Float
OUTnx	
$\overline{\text{RESET}}$	
ASP_DINx	Grounded
CONFIGx	
INnx	
MCLK	
SPI_SDO/I2C_SCL	
SPI_SCK	
SPI_SDI/I2C_SDA	
$\overline{\text{SPI\_CS}}$	Connect to VDD_IO

1.4 Electrostatic Discharge (ESD) Protection

ESD-sensitive device. The CS4282P is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD protection standards.

2 Typical Connection Diagram

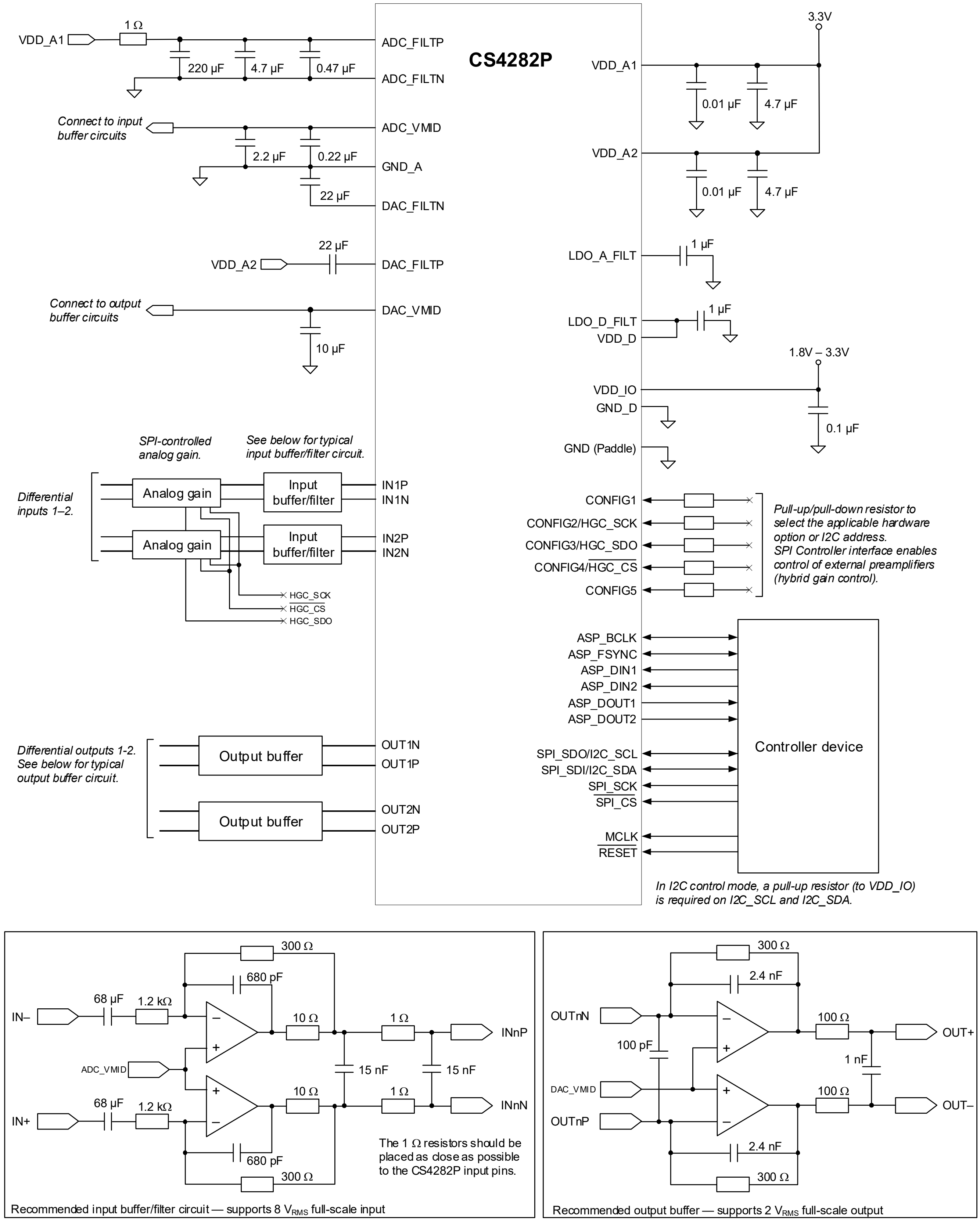


Figure 2-1. Typical Connections

3 Characteristics and Specifications

Note: Table 3-1 defines parameters as they are characterized in this section. Note that default register field configurations are used unless specified otherwise in the test conditions.

Table 3-1. Parameter Definitions

Parameter	Definition
Channel separation	The difference in level between the active channel (driven to maximum full scale output) and the measured signal level in the idle channel at the test signal frequency. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.
Common-mode rejection ratio (CMRR)	The ratio of a specified input signal (applied to both sides of a differential input), relative to the output signal that results from it.
Dynamic range	The difference in level between the maximum full scale output signal and the sum of all harmonic distortion products plus noise with a low-level input signal applied. Typically, an input signal level 60 dB below full scale is used.
Power-supply rejection ratio (PSRR)	The ratio of a specified power supply variation relative to the output signal that results from it. PSRR is measured under quiescent signal path conditions.
Total harmonic distortion plus noise (THD+N)	The ratio of the RMS sum of the harmonic distortion products plus noise in the specified bandwidth relative to the RMS amplitude of the fundamental (i.e., test frequency) output.
Note: Unless specified otherwise, all performance measurements are for a 10 Hz to 20 kHz bandwidth.	

Table 3-2. Recommended Operating Conditions

Test conditions (unless specified otherwise): Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground.

Parameter		Symbol	Minimum	Maximum	Unit
DC power supply	Analog supply [1]	VDDA1, VDDA2	3.13	3.47	V
	Digital supply (powered from internal LDO) [2]	VDD_D	1.14	1.26	V
	Digital I/O supply	VDD_IO	1.71	3.63	V
Supply ramp up/down (all supplies)		$t_{PWR\text{-}UD}$	0.01	10	ms
Ambient temperature		T_A	–40	+85	ºC

Note: The device is fully functional and meets all parametric specifications in this section if operated within the specified conditions. Functionality and parametric performance is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

1. The VDD_A1 and VDD_A2 rails should be tied together and powered from a single supply. The associated power domain is referred to as VDD_A.
2. The digital supply is powered from an internal LDO regulator. The VDD_D pin must be connected to the LDO output pin, LDO_D_FILT.

Table 3-3. Absolute Maximum Ratings

Test conditions (unless specified otherwise): Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground.

Parameter		Symbol	Minimum	Maximum	Unit
DC power supply	Analog supply [1]	VDDA1, VDDA2	–0.3	4.32	V
	Digital supply	VDD_D	–0.3	1.52	V
	Digital I/O supply	VDD_IO	–0.3	4.32	V
External voltage applied to digital input/output		V_{INDI}	–0.3	VDD_IO + 0.3	V
External voltage applied to analog inputs	CONFIG2, CONFIG3, CONFIG4 All other analog inputs	V_{INAI}	–0.3 –0.3	VDD_IO + 0.3 VDD_A + 0.3	V V
Input current	digital input/output analog inputs	I_{in}	— —	±10 ±10	mA mA
Ambient operating temperature		T_A	–40	+115	°C
Junction operating temperature		T_J	–40	+125	°C
Storage temperature		T_{STG}	–65	+150	°C

Caution: Stresses beyond “Absolute Maximum Ratings” levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 3-2 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. The VDD_A1 and VDD_A2 rails should be tied together and powered from a single supply. The associated power domain is referred to as VDD_A.

Table 3-4. ADC Path Characteristics

Test conditions (unless specified otherwise): External components as shown in Fig. 2-1; VDD_A = VDD_IO = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data, MCLK = 24.576 MHz.

Parameter		Min	Typ	Max	Units
Input resistance (INnP to INnN)	Mid impedance (IN12_HIZ = 0) High impedance (IN12_HIZ = 1)	— —	3 100	— —	kΩ kΩ
Full-scale input signal level [1]	0 dBFS output	—	2.0	—	V_{RMS}
Dynamic range	A-weighted unweighted	120 117	123 120	— —	dB dB
THD+N	–1 dBFS output –20 dBFS output –60 dBFS output	— — —	–110 –100 –60	–104 — —	dB dB dB
CMRR	100 mV (peak-peak) 1 kHz	—	80	—	dB
Channel separation		—	110	—	dB
Interchannel phase deviation		—	0.03	—	degree
Interchannel gain deviation		—	0.1	—	dB
Gain drift		—	±100	—	ppm/°C
PSRR (VDD_A)	100 mV (peak-peak) 1 kHz sine wave	—	65	—	dB

1.The full-scale input signal level is also the maximum analog input level, before clipping occurs. A sinusoidal input signal is assumed. Full-scale input signal level scales with VDD_A.

Table 3-5. DAC Path Characteristics

Test conditions (unless specified otherwise): External components as shown in Fig. 2-1; VDD_A = VDD_IO = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND_A = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data, MCLK = 24.576 MHz; measured with output connected to a 300 Ω transimpedance amplifier as shown in Fig. 2-1.

Parameter		Min	Typ	Max	Units
Full scale output	0 dBFS input	—	6.67		mA_{RMS}
Dynamic range	A-weighted unweighted	125 122	128 125	— —	dB dB
THD+N	0 dBFS input –20 dBFS input –60 dBFS input	— — —	–115 –103 –63	TBD — —	dB dB dB
Idle channel noise	A-weighted	—	2.45	—	nA_{RMS}
Channel separation	1 kHz 20 kHz	— —	110 100	— —	dB dB
PSRR (VDD_A)	100 mV (peak-peak) 1 kHz sine wave	—	75	—	dB

Table 3-6. ADC Filter Characteristics

Test conditions (unless specified otherwise): VDD_A = VDD_IO = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC; 1 kHz sine wave test signal, 32-bit audio data.

Parameter				Min	Typ	Max	Units
Fs = 32 kHz	Fast roll-off	Passband	to –3 dB corner	—	—	0.47	Fs
		Passband ripple	f ≤ 0.45 Fs	–0.092	—	0.092	dB
		Stopband attenuation	f ≥ 0.55 Fs	98	—	—	dB
		Group delay [1]	linear phase minimum phase	— —	20.5/Fs 4.1/Fs	— —	s s
Fs = 44.1 or 48 kHz	Fast roll-off	Passband	to –3 dB corner	—	—	0.48	Fs
		Passband ripple	f ≤ 0.46 Fs	–0.011	—	0.011	dB
		Stopband attenuation	f ≥ 0.54 Fs	98	—	—	dB
		Group delay [1]	linear phase minimum phase	— —	27.6/Fs 4.0/Fs	— —	s s
	Slow roll-off	Passband	to –3 dB corner	—	—	0.46	Fs
		Passband ripple	f ≤ 0.42 Fs	–0.099	—	0.099	dB
		Stopband attenuation	f ≥ 0.58 Fs	96	—	—	dB
		Group delay [1]	linear phase minimum phase	— —	13.3/Fs 3.9/Fs	— —	s s

Table 3-6. ADC Filter Characteristics *(Cont.)*

Test conditions (unless specified otherwise): VDD_A = VDD_IO = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC; 1 kHz sine wave test signal, 32-bit audio data.

Parameter				Min	Typ	Max	Units
Fs = 88.2 or 96 kHz	Fast roll-off	Passband	to –3 dB corner	—	—	0.48	Fs
		Passband ripple	f ≤ 0.45 Fs	–0.006	—	0.006	dB
		Stopband attenuation	f ≥ 0.55 Fs	111	—	—	dB
		Group delay [1]	linear phase minimum phase	— —	32.3/Fs 6.3/Fs	— —	s s
	Slow roll-off	Passband	to –3 dB corner	—	—	0.43	Fs
		Passband ripple	f ≤ 0.27 Fs	–0.011	—	0.011	dB
		Stopband attenuation	f ≥ 0.77 Fs	103	—	—	dB
		Group delay [1]	linear phase minimum phase	— —	7.0/Fs 4.1/Fs	— —	s s
Fs = 176.4 or 192 kHz	Fast roll-off	Passband	to –3 dB corner	—	—	0.47	Fs
		Passband ripple	f ≤ 0.43 Fs	–0.009	—	0.009	dB
		Stopband attenuation	f ≥ 0.57 Fs	99	—	—	dB
		Group delay [1]	linear phase minimum phase	— —	19.1/Fs 5.2/Fs	— —	s s
	Slow roll-off	Passband	to –3 dB corner	—	—	0.29	Fs
		Passband ripple	f ≤ 0.12 Fs	–0.010	—	0.010	dB
		Stopband attenuation	f ≥ 0.67 Fs	99	—	—	dB
		Group delay [1]	linear phase minimum phase	— —	6.4/Fs 4.2/Fs	— —	s s
Fs = 352.8 or 384 kHz	Fast roll-off	Passband	to –3 dB corner	—	—	0.48	Fs
		Passband ripple	f ≤ 0.43 Fs	–0.010	—	0.010	dB
		Stopband attenuation	f ≥ 0.57 Fs	100	—	—	dB
		Group delay [1]	linear phase minimum phase	— —	23.8/Fs 7.5/Fs	— —	s s
	Slow roll-off	Passband	to –3 dB corner	—	—	0.34	Fs
		Passband ripple	f ≤ 0.06 Fs	–0.001	—	0.001	dB
		Stopband attenuation	f ≥ 0.94 Fs	129	—	—	dB
		Group delay [1]	linear phase minimum phase	— —	5.8/Fs 4.7/Fs	— —	s s
Fs = 705.6 or 768 kHz	Fast roll-off	Passband	to –3 dB corner	—	—	0.38	Fs
		Passband ripple	f ≤ 0.22 Fs	–0.009	—	0.009	dB
		Stopband attenuation	f ≥ 0.78 Fs	118	—	—	dB
		Group delay [1]	linear phase minimum phase	— —	9.1/Fs 6.4/Fs	— —	s s
	Slow roll-off	Passband	to –3 dB corner	—	—	0.30	Fs
		Passband ripple	f ≤ 0.03 Fs	–0.008	—	0.008	dB
		Stopband attenuation	f ≥ 0.97 Fs	119	—	—	dB
		Group delay [1]	linear phase minimum phase	— —	7.1/Fs 6.2/Fs	— —	s s

1. Group delay is measured from the time at which a signal is presented on the input pins (INnP/INnN) to the time of the first data bit of the corresponding FSYNC frame being output on the ASP_DOUTn pin.

Table 3-7. ADC High-Pass Filter (HPF)

Test conditions (unless specified otherwise): VDD_A = VDD_IO = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data.

Parameter		Min	Typ	Max	Units
Passband	–0.01 dB corner –3 dB corner	— —	19 1	— —	Hz Hz
Phase deviation	f = 20 Hz	—	0.001	—	degree
Filter settling time		—	0.4	—	s

Table 3-8. DAC Filter Characteristics

Test conditions (unless specified otherwise): VDD_A = VDD_IO = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND_A = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data.

Parameter				Min	Typ	Max	Units
Fs = 32 kHz	Fast roll-off	Passband	to –3 dB corner	—	—	0.49	Fs
		Passband ripple	f ≤ 0.45 Fs	–0.001	—	0.001	dB
		Stopband attenuation	f ≥ 0.55 Fs	100	—	—	dB
		Group delay [1]	linear phase minimum phase	— —	32.5/Fs 4.6/Fs	— —	s s
Fs = 44.1 or 48 kHz	Fast roll-off	Passband	to –3 dB corner	—	—	0.49	Fs
		Passband ripple	f ≤ 0.45 Fs	–0.001	—	0.001	dB
		Stopband attenuation	f ≥ 0.55 Fs	100	—	—	dB
		Group delay [1]	linear phase minimum phase	— —	32.6/Fs 4.7/Fs	— —	s s
	Slow roll-off	Passband	to –3 dB corner	—	—	0.47	Fs
		Passband ripple	f ≤ 0.42 Fs	–0.004	—	0.005	dB
		Stopband attenuation	f ≥ 0.59 Fs	101	—	—	dB
		Group delay [1]	linear phase minimum phase	— —	17.1/Fs 4.6/Fs	— —	s s
Fs = 88.2 or 96 kHz	Fast roll-off	Passband	to –3 dB corner	—	—	0.49	Fs
		Passband ripple	f ≤ 0.45 Fs	–0.001	—	0.001	dB
		Stopband attenuation	f ≥ 0.55 Fs	101	—	—	dB
		Group delay [1]	linear phase minimum phase	— —	32.9/Fs 5.0/Fs	— —	s s
	Slow roll-off	Passband	to –3 dB corner	—	—	0.39	Fs
		Passband ripple	f ≤ 0.23 Fs	–0.005	—	0.005	dB
		Stopband attenuation	f ≥ 0.70 Fs	90	—	—	dB
		Group delay [1]	linear phase minimum phase	— —	7.4/Fs 4.5/Fs	— —	s s
	Balanced roll-off	Passband	to –3 dB corner	—	—	0.35	Fs
		Passband ripple	f ≤ 0.23 Fs	–0.001	—	0.001	dB
		Stopband attenuation	f ≥ 0.55 Fs	101	—	—	dB
		Group delay [1]	linear phase minimum phase	— —	11.6/Fs 5.2/Fs	— —	s s
Fs = 176.4 or 192 kHz	Fast roll-off	Passband	to –3 dB corner	—	—	0.48	Fs
		Passband ripple	f ≤ 0.45 Fs	–0.004	—	0.005	dB
		Stopband attenuation	f ≥ 0.55 Fs	103	—	—	dB
		Group delay [1]	linear phase minimum phase	— —	35.1/Fs 6.6/Fs	— —	s s
	Slow roll-off	Passband	to –3 dB corner	—	—	0.36	Fs
		Passband ripple	f ≤ 0.11 Fs	–0.001	—	0.001	dB
		Stopband attenuation	f ≥ 0.80 Fs	108	—	—	dB
		Group delay [1]	linear phase minimum phase	— —	7.6/Fs 5.4/Fs	— —	s s
	Balanced roll-off	Passband	to –3 dB corner	—	—	0.28	Fs
		Passband ripple	f ≤ 0.11 Fs	–0.001	—	0.001	dB
		Stopband attenuation	f ≥ 0.55 Fs	110	—	—	dB
		Group delay [1]	linear phase minimum phase	— —	10.6/Fs 6.7/Fs	— —	s s
Fs = 352.8 or 384 kHz	Fast roll-off	Passband	to –3 dB corner	—	—	0.30	Fs
		Passband ripple	f ≤ 0.23 Fs	–0.004	—	0.000	dB
		Stopband attenuation	f ≥ 0.55 Fs	116	—	—	dB
		Group delay [1]	linear phase minimum phase	— —	14.4/Fs 7.7/Fs	— —	s s
	Balanced roll-off	Passband	to –3 dB corner	—	—	0.23	Fs
		Passband ripple	f ≤ 0.06 Fs	–0.001	—	0.000	dB
		Stopband attenuation	f ≥ 0.55 Fs	116	—	—	dB
		Group delay [1]	linear phase minimum phase	— —	10.4/Fs 7.6/Fs	— —	s s

Table 3-8. DAC Filter Characteristics *(Cont.)*

Test conditions (unless specified otherwise): VDD_A = VDD_IO = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND_A = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data.

Parameter				Min	Typ	Max	Units
Fs = 705.6 or 768 kHz	Fast roll-off	Passband	to –3 dB corner	—	—	0.15	Fs
		Passband ripple	f ≤ 0.11 Fs	–0.005	—	0.001	dB
		Stopband attenuation	f ≥ 0.30 Fs	101	—	—	dB
		Group delay [1]	linear phase minimum phase	— —	23.9/Fs 13.7/Fs	— —	s s
	Balanced roll-off	Passband	to –3 dB corner	—	—	0.12	Fs
		Passband ripple	f ≤ 0.03 Fs	–0.001	—	0.000	dB
		Stopband attenuation	f ≥ 0.27 Fs	116	—	—	dB
		Group delay [1]	linear phase minimum phase	— —	19.9/Fs 14.3/Fs	— —	s s

1. Group delay is measured from the start of the FSYNC frame containing the audio data on the ASP_DINn pin to the time at which the signal is presented on the output pins (OUTnP/OUTnN).

Table 3-9. DAC High-Pass Filter (HPF)

Test conditions (unless specified otherwise): VDD_A = VDD_IO = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND_A = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data.

Parameter		Min	Typ	Max	Units
Passband	–0.01 dB corner –3 dB corner	— —	19 1	— —	Hz Hz
Phase deviation	f = 20 Hz	—	0.001	—	degree
Filter settling time		—	0.4	—	s

Table 3-10. Device Power Consumption

Test conditions (unless specified otherwise): VDD_A = VDD_IO = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data.

Use Configuration		Typical Current (mA)		Total Power (mW)
		I_{VDD_A}	I_{VDD_IO}	
Reset	$\overline{RESET}$ = Logic 0	0.70	0.04	2.4
Two ADC + two DAC channels enabled	Mid impedance (IN12_HIZ = 0) High impedance (IN12_HIZ = 1)	TBD TBD	TBD TBD	TBD TBD

Table 3-11. Digital Interface Specifications and Characteristics

Test conditions (unless specified otherwise): Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC.

Parameter		Symbol	Minimum	Maximum	Unit
Input leakage current (per pin)		I_{IN}	—	±10	µA
Input capacitance (per pin)		—	—	5	pF
Digital I/O (VDD_IO logic—all pins except CONFIG1 and CONFIG5) [1]	High-level output	V_{OH}	0.9×VDD_IO	—	V
	Low-level output	V_{OL}	—	0.1×VDD_IO	V
	High-level input	V_{IH}	0.7×VDD_IO	—	V
	Low-level input	V_{IL}	—	0.3×VDD_IO	V
Digital I/O (VDD_A logic—CONFIG1 and CONFIG5 pins) [1]	High-level output	V_{OH}	0.9×VDD_A	—	V
	Low-level output	V_{OL}	—	0.1×VDD_A	V

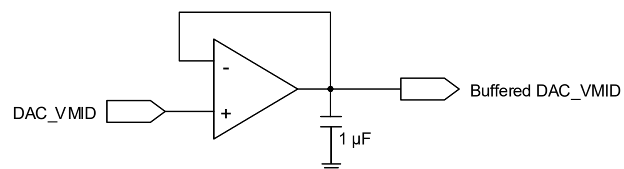
1. The CONFIG2, CONFIG3, and CONFIG4 pins are configured as digital output if HGC_SPI_EN is set; this is used to support the hybrid gain control (see Section 4.5.4). The CONFIGx pins also support digital output if configured as GP output (see Section 4.10).

Table 3-12. DC Characteristics

Test conditions (unless specified otherwise): VDD_A = VDD_IO = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC.

Parameter			Minimum	Typical	Maximum	Unit
DAC_FILT [1]	Nominal voltage	VDD_A to DAC_FILTP DAC_FILTN to GND	— —	2.00 1.25	— —	V V
	Maximum output current		—	50	—	µA
DAC_VMID [2]	Nominal voltage		—	1.65	—	V
	Maximum output current		—	0.01	—	mA
ADC_FILT [3]	Nominal voltage		—	3.3	—	V
	Maximum output current		—	0.01	—	mA
ADC_VMID [4]	Nominal voltage		—	1.65	—	V
	Maximum output current		—	0.01	—	mA
VDD_A power-on reset (POR) threshold (V_{POR})		VDD_A rising VDD_A falling	1.9 1.8	— —	2.7 2.6	V V
VDD_D power-on reset (POR) threshold (V_{POR})		VDD_D rising VDD_D falling	0.90 0.75	— —	1.05 0.90	V V

1. DAC_FILT characteristics are provided as a guide for external component selection. The output current (arising from capacitor leakage) must be less than the maximum output current of the DAC_FILT pin.
2. The output current (arising from capacitor leakage and the input-buffer circuit) must be less than the maximum output current of the DAC_VMID pin. If a larger current is required, an external VMID buffer should be used. A buffer can be provided using a standard op-amp (noise voltage < 5 nV/√Hz, input current < 10 µA). An example circuit is as follows:



3. ADC_FILT characteristics are measured between ADC_FILTP and ADC_FILTN, and are provided as a guide for external component selection. The output current (arising from capacitor leakage) must be less than the maximum output current of the ADC_FILT pin.
4. The output current (arising from capacitor leakage and the input-buffer circuit) must be less than the maximum output current of the ADC_VMID pin. If a larger current is required, an external VMID buffer should be used. A buffer can be provided using a standard op-amp (noise voltage < 5 nV/√Hz, input current < 10 µA). An example circuit is as follows:

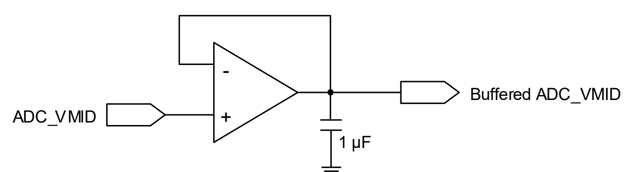


Table 3-13. Switching Specifications—Reset and Clock References

Test conditions (unless specified otherwise): VDD_A = VDD_IO = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC.

Parameter		Symbol	Minimum	Typical	Maximum	Unit
Reset	$\overline{\text{RESET}}$ low (logic 0) pulse width	t_{RLPW}	1	—	—	ms
	$\overline{\text{RESET}}$ rising edge to control port active	t_{IRS}	—	—	5	ms
MCLK input	MCLK frequency (MCLK as clock source, PLL not used)	f_{MCLK}	— —	45.1584 49.152	— —	MHz MHz
	MCLK duty cycle (MCLK as clock source, PLL not used)	D_{MCLK}	40	—	60	%
	MCLK frequency tolerance (MCLK as clock source, PLL not used)	—	–1	—	1	%
Phase-locked loop (PLL)	REFCLK input frequency (BCLK or MCLK reference) [1]	f_{REFCLK}	— — — — — — — —	2.8224 5.6448 11.2896 22.5792 3.072 6.144 12.288 24.576	— — — — — — — —	MHz MHz MHz MHz MHz MHz MHz MHz
	REFCLK input duty cycle	D_{REFCLK}	45	—	55	%
	REFCLK frequency tolerance	—	–1	—	1	%
	PLL output frequency Fs = 32, 48, 96, 192, 384, 768 kHz Fs = 44.1, 88.2, 176.4, 352.8, 705.6 kHz	f_{PLL_OUT}	— —	49.152 45.1584	— —	MHz MHz
	PLL output jitter	j_{PLL_OUT}	—	500	—	ps_{RMS}
	PLL output period jitter	$j_{PLL\_OUT\text{-}PER}$	—	—	500	ps
	PLL lock time	t_{PLL_LOCK}	—	0.3	1	ms

1.Note the REFCLK input frequency must be integer-related to the sample rate. See Section 4.4 for further details.

Table 3-14. Switching Specifications—Audio Serial Port (ASP)

Test conditions (unless specified otherwise): VDD_A = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO logic (as specified in Table 3-11); T_A = 25°C.

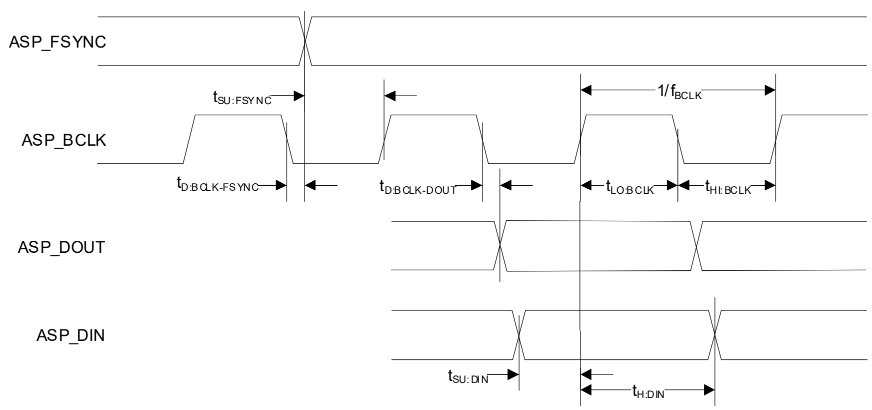
Parameter [1,2,3,4,5]			Symbol	Minimum	Maximum	Unit
Secondary Mode, VDD_IO = 3.3 V	ASP_FSYNC input sample/frame rate		Fs	32	768	kHz
	ASP_FSYNC pulse width		$t_{HI:FSYNC}$	$1/f_{ASP\_BCLK}$	—	ns
	ASP_BCLK frequency		f_{BCLK}	2.048	24.576	MHz
	ASP_BCLK high period		$t_{HI:BCLK}$	18	—	ns
	ASP_BCLK low period		$t_{LO:BCLK}$	18	—	ns
	ASP_FSYNC setup time before ASP_BCLK latching edge		$t_{SU:FSYNC}$	5	—	ns
	ASP_FSYNC hold time after ASP_BCLK latching edge		$t_{H:FSYNC}$	5	—	ns
	ASP_DIN setup time before ASP_BCLK latching edge		$t_{SU:DIN}$	10	—	ns
	ASP_DIN hold time after ASP_BCLK latching		$t_{H:DIN}$	5	—	ns
	ASP_DOUT delay after ASP_BCLK launching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	$t_{D:BCLK–DOUT}$	0 0	10 12	ns ns
	ASP_DOUT Hi-Z delay after ASP_BCLK latching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	$t_{DLY:HiZ}$	0 0	9 9	ns ns
	ASP_DOUT delay from Hi-Z after ASP_BCLK launching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	$t_{DLY:EN}$	0 10	10 28	ns ns
	ASP_x load capacitance	ASP_DOUTx	—	0	150	pF
Primary Mode, VDD_IO = 3.3 V	ASP_FSYNC output sample/frame rate		Fs	32	768	kHz
	ASP_BCLK frequency		f_{BCLK}	2.8224	24.576	MHz
	ASP_BCLK duty cycle	PLL enabled, MCLK duty cycle 40–60% PLL bypass, BCLK < 22.5792 MHz, MCLK 40–60% PLL bypass, BCLK ≥ 22.5792 MHz, MCLK 45–55% PLL bypass, BCLK ≥ 22.5792 MHz, MCLK 40–60%	D_{BCLK}	45 45 42 37	55 55 58 63	% % % %
	ASP_FSYNC delay time after ASP_BCLK launching edge		$t_{D:BCLK–FSYNC}$	0	20	ns
	ASP_DIN setup time before ASP_BCLK latching edge		$t_{SU:DIN}$	6	—	ns
	ASP_DIN hold time after ASP_BCLK latching edge		$t_{H:DIN}$	5	—	ns
	ASP_DOUT delay after ASP_BCLK launching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	$t_{D:BCLK–DOUT}$	0 0	11 13	ns ns
	ASP_DOUT Hi-Z delay after ASP_BCLK latching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	$t_{DLY:HiZ}$	0 0	10 10	ns ns
	ASP_DOUT delay from Hi-Z after ASP_BCLK launching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	$t_{DLY:EN}$	0 7	15 28	ns ns
	ASP_x load capacitance	ASP_BCLK ASP_FSYNC ASP_DOUTx	—	0 0 0	50 50 150	pF pF pF
Secondary Mode, VDD_IO = 1.8 V	ASP_FSYNC input sample/frame rate		Fs	32	768	kHz
	ASP_FSYNC pulse width		$t_{HI:FSYNC}$	$1/f_{ASP\_BCLK}$	—	ns
	ASP_BCLK frequency		f_{BCLK}	2.048	24.576	MHz
	ASP_BCLK high period		$t_{HI:BCLK}$	18	—	ns
	ASP_BCLK low period		$t_{LO:BCLK}$	18	—	ns
	ASP_FSYNC setup time before ASP_BCLK latching edge		$t_{SU:FSYNC}$	5	—	ns
	ASP_FSYNC hold time after ASP_BCLK latching edge		$t_{H:FSYNC}$	5	—	ns
	ASP_DIN setup time before ASP_BCLK latching edge		$t_{SU:DIN}$	10	—	ns
	ASP_DIN hold time after ASP_BCLK latching		$t_{H:DIN}$	5	—	ns
	ASP_DOUT delay after ASP_BCLK launching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	$t_{D:BCLK–DOUT}$	0 0	15 17	ns ns
	ASP_DOUT Hi-Z delay after ASP_BCLK latching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	$t_{DLY:HiZ}$	0 0	12 12	ns ns
	ASP_DOUT delay from Hi-Z after ASP_BCLK launching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	$t_{DLY:EN}$	0 11	15 33	ns ns
	ASP_x load capacitance	ASP_DOUTx	—	0	150	pF

Table 3-14. Switching Specifications—Audio Serial Port (ASP) *(Cont.)*

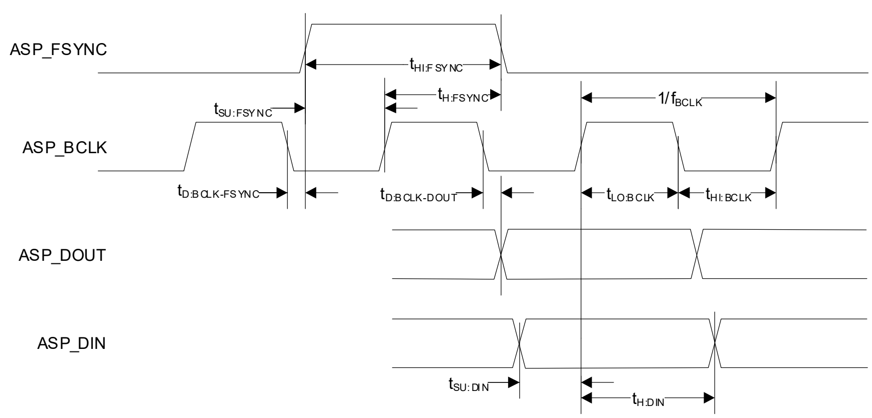
Test conditions (unless specified otherwise): VDD_A = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO logic (as specified in Table 3-11); T_A = 25°C.

Parameter [1,2,3,4,5]			Symbol	Minimum	Maximum	Unit
Primary Mode, VDD_IO = 1.8 V	ASP_FSYNC output sample/frame rate		Fs	32	768	kHz
	ASP_BCLK frequency		f_{BCLK}	2.8224	24.576	Mhz
	ASP_BCLK duty cycle	PLL enabled, MCLK duty cycle 40–60% PLL bypass, BCLK < 22.5792 MHz, MCLK 40–60% PLL bypass, BCLK ≥ 22.5792 MHz, MCLK 45–55% PLL bypass, BCLK ≥ 22.5792 MHz, MCLK 40–60%	D_{BCLK}	45 45 42 37	55 55 58 63	% % % %
	ASP_FSYNC delay time after ASP_BCLK launching edge		$t_{D:BCLK–FSYNC}$	0	20	ns
	ASP_DIN setup time before ASP_BCLK latching edge		$t_{SU:DIN}$	6	—	ns
	ASP_DIN hold time after ASP_BCLK latching edge		$t_{H:DIN}$	5	—	ns
	ASP_DOUT delay after ASP_BCLK launching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	$t_{D:BCLK–DOUT}$	0 0	16 18	ns ns
	ASP_DOUT Hi-Z delay after ASP_BCLK latching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	$t_{DLY:HiZ}$	0 0	13 13	ns ns
	ASP_DOUT delay from Hi-Z after ASP_BCLK launching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	$t_{DLY:EN}$	0 7	15 34	ns ns
	ASP_x load capacitance	ASP_BCLK ASP_FSYNC ASP_DOUTx	—	0 0 0	50 50 150	pF pF pF

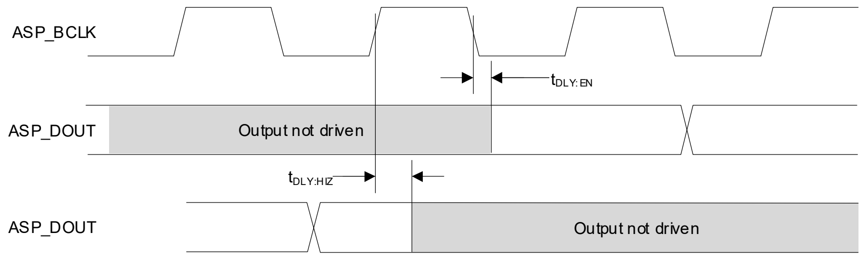
1. The ASP_BCLK launching edge is selectable. Half-cycle mode = ASP_BCLK launching edge is opposite to latching edge. Full-cycle mode = ASP_BCLK launching edge is same as latching edge.
2. ASP timing in I²S and Left-Justified Modes.
   Note that ASP_BCLK can be inverted if required; the figure shows the default polarity in half-cycle mode.



3. ASP timing in TDM Mode.
   Note that ASP_BCLK can be inverted if required; the figure shows the default polarity in half-cycle mode.



4. ASP_DOUT timing for multiple devices sharing the audio serial port bus—half-cycle mode.



5. ASP_DOUT timing for multiple devices sharing the audio serial port bus—full-cycle mode.

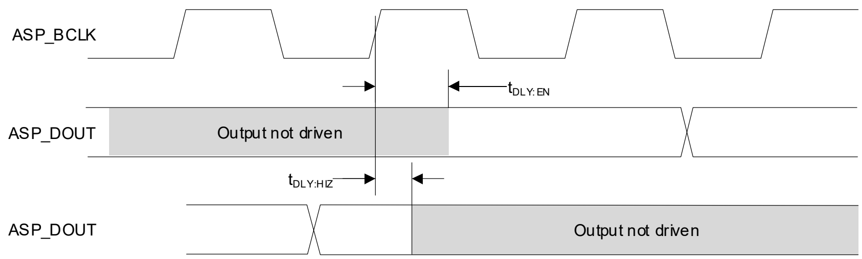


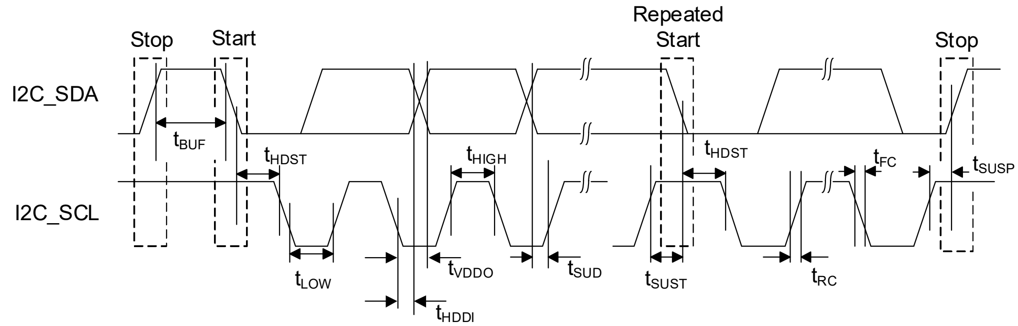
Table 3-15. Switching Specifications—I²C Control Port

Test conditions (unless specified otherwise): VDD_A = VDD_IO = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO logic (as specified in Table 3-11); T_A = 25°C.

Parameter [1,2]		Symbol	Minimum	Maximum	Unit
SCL clock frequency		f_{SCL}	—	1000	kHz
Clock low time		t_{LOW}	500	—	ns
Clock high time		t_{HIGH}	260	—	ns
Start condition hold time (before first clock pulse)		t_{HDST}	260	—	ns
Setup time for repeated start		t_{SUST}	260	—	ns
Rise time of SCL and SDA	f_{SCL} ≤ 100 kHz 100 kHz < f_{SCL} ≤ 400 kHz 400 kHz < f_{SCL} ≤ 1000 kHz	t_{RC}	600 180 72	1000 300 120	ns ns ns
Fall time of SCL and SDA	f_{SCL} ≤ 100 kHz 100 kHz < f_{SCL} ≤ 400 kHz 400 kHz < f_{SCL} ≤ 1000 kHz	t_{FC}	6.5 6.5 6.5	300 300 120	ns ns ns
Rise time variation between SDA and SCL		—	—	1.67	x
Fall time variation between SDA and SCL	f_{SCL} ≤ 100 kHz 100 kHz < f_{SCL} ≤ 400 kHz 400 kHz < f_{SCL} ≤ 1000 kHz	—	— — —	100 100 75	ns ns ns
Setup time for stop condition		t_{SUSP}	260	—	ns
SDA setup time to SCL rising		t_{SUD}	50	—	ns
SDA input hold time from SCL falling [3]		t_{HDDI}	0	—	ns
Output data valid (Data/ACK) [4]	f_{SCL} ≤ 100 kHz 100 kHz < f_{SCL} ≤ 400 kHz 400 kHz < f_{SCL} ≤ 1000 kHz	t_{VDDO}	— — —	3450 900 450	ns ns ns
Bus free time between transmissions		t_{BUF}	500	—	ns
SDA bus capacitance		C_B	—	550	pF
SCL/SDA pull-up resistance		R_P	500	—	Ω
Pulse width of spikes to be suppressed		t_{ps}	0	50	ns

1. All timing is relative to thresholds specified in Table 3-11, V_{IL} and V_{IH} for input signals, and V_{OL} and V_{OH} for output signals.

2. I²C control-port timing.



3. Data must be held long enough to bridge the transition time, t_{FC}, of SCL.
4. Time from falling edge of SCL until data output is valid.

Table 3-16. Switching Specifications—SPI Control Port

Test conditions (unless specified otherwise): VDD_A = VDD_IO = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO logic (as specified in Table 3-11); T_A = 25°C.

Parameter [1]	Symbol	Minimum	Maximum	Unit
SPI_SCK frequency	f_{SCY}	—	24	MHz
SPI_CS falling edge to SPI_SCK rising edge	t_{SSU}	5	—	ns
SPI_SCK falling edge to SPI_CS rising edge	t_{SHO}	0.5	—	ns
SPI_SCK pulse width low	t_{SCL}	18.5	—	ns
SPI_SCK pulse width high	t_{SCH}	18.5	—	ns
SPI_SDI to SPI_SCK setup time	t_{DSU}	5	—	ns
SPI_SDI to SPI_SCK hold time	t_{DHO}	2.5	—	ns
SPI_SCK falling edge to SPI_SDO transition	t_{DL}	0	15	ns
SPI_CS rising edge to SPI_SDO output high-Z	—	0	15	ns
Bus free time between active SPI_CS	t_{SH}	20	—	ns

1. SPI control-port timing.

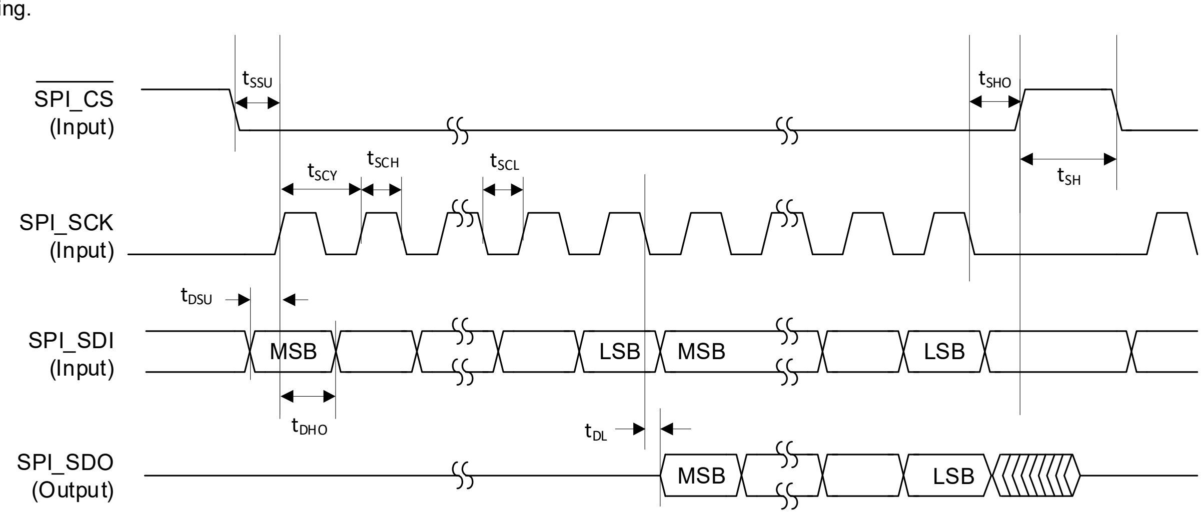
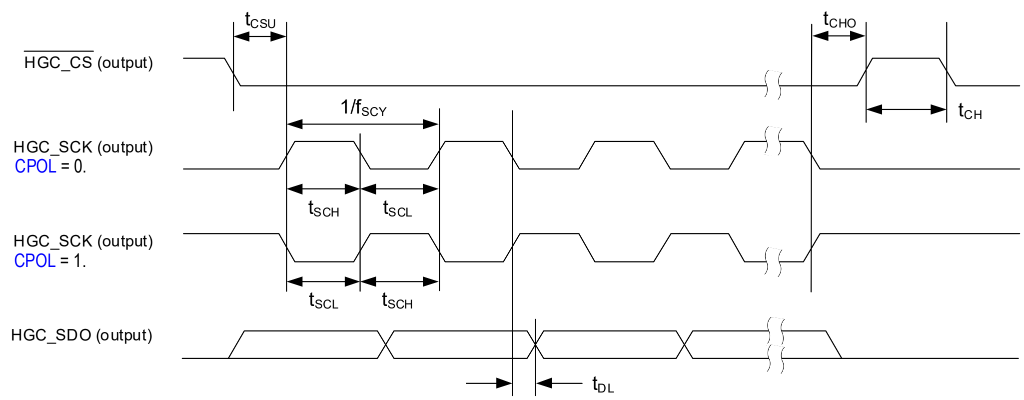


Table 3-17. Switching Specifications—SPI Controller (Hybrid Gain Control)

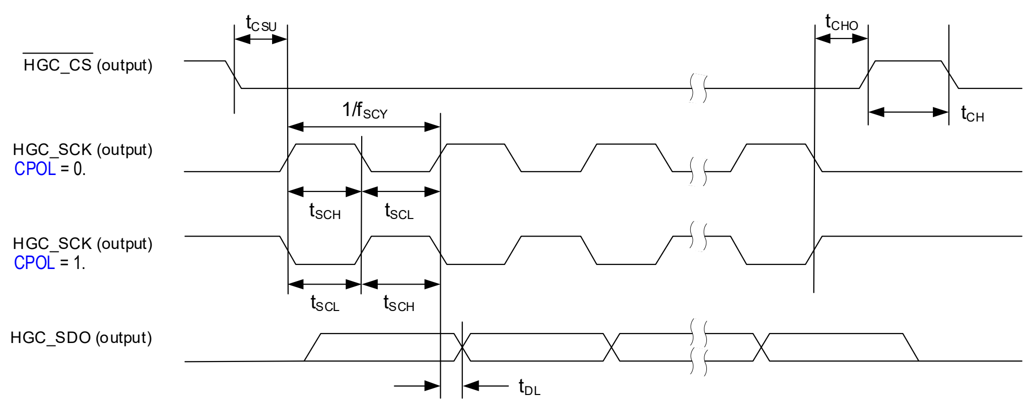
Test conditions (unless specified otherwise): VDD_A = VDD_IO = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground; output timings are measured at V_{OL} and V_{OH} thresholds for VDD_A logic (as specified in Table 3-11); T_A = 25°C.

Parameter [1,2]		Symbol	Minimum	Maximum	Unit
HGC_SCK frequency		f_{SCY}	—	12.288	MHz
$\overline{\text{HGC\_CS}}$ falling edge to HGC_SCK rising edge		t_{CSU}	30	—	ns
HGC_SCK falling edge to $\overline{\text{HGC\_CS}}$ rising edge		t_{CHO}	30	—	ns
HGC_SCK pulse width low		t_{SCL}	40	—	ns
HGC_SCK pulse width high		t_{SCH}	40	—	ns
HGC_SCK falling edge to HGC_SDO transition	C_{LOAD} (HGC_SDO) = 30 pF C_{LOAD} (HGC_SDO) = 60 pF	t_{DL}	–15 –20	15 20	ns ns

1.SPI Master timing, CPHA = 0.



2.SPI Master timing, CPHA = 1.



4 Functional Description

4.1 Device Power and Reset

The CS4282P is powered using VDD_A1, VDD_A2, VDD_D, and VDD_IO external supplies.

Notes: The VDD_A1 and VDD_A2 rails should be tied together and powered from a single supply. The associated power domain is referred to as VDD_A.

The digital supply, VDD_D, is powered from an internal LDO regulator. The output of the LDO regulator is provided on the LDO_D_FILT pin—the VDD_D pin should be connected to LDO_D_FILT.

There are no power-sequencing requirements—supplies can be enabled in any order.

The CS4282P is in reset if the $\overline{\text{RESET}}$ pin is asserted (Logic 0), or if the VDD_A or VDD_D supply is below the respective reset threshold defined in Table 3-12.

All ground pins, including the ground paddle, must be tied to a common ground plane directly underneath the CS4282P.

4.2 Hardware Configuration

The CS4282P supports hardware and software control modes. In hardware mode, the device configuration is determined entirely by external resistors connected to the hardware-control pins. In software mode, the I^{2}C/SPI control port is used to configure the device.

Note: The hardware-control pins CONFIG1 and CONFIG5 are powered by VDD_A. The CONFIG2, CONFIG3, and CONFIG4 pins are powered by VDD_IO. Care must be taken to ensure any external pull-up resistors on these pins are connected to the applicable power domain.

In hardware mode, the audio serial port (ASP) configuration is selected using the CONFIG1 and CONFIG2 pins as described in Table 4-1. See Section 4.4 for more details of the sample-rate selection. See Section 4.8 for more details of the ASP operation.

Table 4-1. Hardware Control—ASP Configuration

Pin Name	Pin Configuration		Description
CONFIG1	Pull-up to VDD_A	0 Ω	Software control mode (I^{2}C/SPI)
		4.7 kΩ	ASP Primary Mode, 44.1 kHz, 48 kHz sample rate
		22 kΩ	ASP Primary Mode, 88.2 kHz, 96 kHz sample rate
		100 kΩ	ASP Primary Mode, 176.4 kHz, 192 kHz sample rate
	Pull-down to GND_A	100 kΩ	ASP Secondary Mode, 176.4 kHz, 192 kHz sample rate
		22 kΩ	ASP Secondary Mode, 88.2 kHz, 96 kHz sample rate
		4.7 kΩ	ASP Secondary Mode, 44.1 kHz, 48 kHz sample rate
		0 Ω	ASP Secondary Mode, autodetect sample rate [1,2]
CONFIG2	Pull-up to VDD_IO	0 Ω	ASP TDM Mode—minimum time slots [3]
		4.7 kΩ	ASP TDM Mode—maximum time slots [4], data output on BCLK falling edge (half-cycle mode) [5]
		22 kΩ	ASP TDM Mode—maximum time slots [4], data output on BCLK rising edge (full-cycle mode) [6]
		100 kΩ	—
	Pull-down to GND_D	100 kΩ	—
		22 kΩ	—
		4.7 kΩ	ASP Left-Justified Mode
		0 Ω	ASP I^{2}S Mode

1. Valid sample rates for autodetect are 32, 44.1, 48, 88.2, 96, 176.4, and 192 kHz.
2. Autodetect sample rate is only supported in MCLK = 256 fs(base), MCLK = 512 fs(base), or MCLK 1024 fs(base) clocking configurations (see Table 4-3).
3. The ASP data format is configured to support the minimum number of time slots necessary for the 2-channel CS4282P input/output.
4. The ASP data format is configured to support the maximum number of time slots for the applicable BCLK rate.
5. Half-cycle mode = ASP_DOUT launching edge (BCLK falling) is opposite to the receiving-device latching edge (BCLK rising).
6. Full-cycle mode = ASP_DOUT launching edge (BCLK rising) is same as the receiving-device latching edge.

If the ASP is configured for TDM data format with maximum time slots, the TDM slot selection is determined using the CONFIG3 pin as described in Table 4-2. See Section 4.8 for more details of the ASP TDM modes.

Table 4-2. Hardware Control—TDM Slot Selection

Pin Name	Pin Configuration		Description
CONFIG3	Pull-up to VDD_IO	0 Ω	Slots 14–15 [1]
		4.7 kΩ	Slots 12–13 [1]
		22 kΩ	Slots 10–11 [1]
		100 kΩ	Slots 8–9 [1]
	Pull-down to GND_D	100 kΩ	Slots 6–7 [2]
		22 kΩ	Slots 4–5 [2]
		4.7 kΩ	Slots 2–3
		0 Ω	Slots 0–1

1. Slots 8–15 are only valid in 16-slot TDM Mode.
2. Slots 4–7 are only valid in 8-slot or 16-slot TDM Mode.

The clock-reference configuration is determined using the CONFIG4 pin as described in Table 4-3. See Section 4.4 for more details of the CS4282P clocking architecture.

Table 4-3. Hardware Control—Clocking Configuration

Pin Name	Pin Configuration		Clock Reference [1,2,3,4]	PLL
CONFIG4	Pull-up to VDD_IO	0 Ω	BCLK = 64 fs	Enabled
		4.7 kΩ	MCLK = 1024 fs(base)	Bypass
		22 kΩ	MCLK = 256 fs(base)	Enabled
		100 kΩ	MCLK = 512 fs(base)	Enabled
	Pull-down to GND_A	100 kΩ	MCLK = 512 fs(base)	Enabled
		22 kΩ	MCLK = 256 fs(base)	Enabled
		4.7 kΩ	MCLK = 1024 fs(base)	Bypass
		0 Ω	BCLK = 64 fs	Enabled

1. fs = sample rate, 44.1, 48, 88.2, 96, 176.4, or 192 kHz.
2. fs(base) is the base sample rate. fs(base) = 48 kHz for 48 kHz-related sample rates; fs(base) = 44.1 kHz for 44.1 kHz-related sample rates.
3. BCLK 64 fs configuration is only supported in ASP Secondary Mode.
4. Autodetect sample rate (see Table 4-1) is only supported in MCLK = 256 fs(base), MCLK = 512 fs(base), or MCLK 1024 fs(base) clocking configurations.

In hardware mode, the digital filter is selected using the CONFIG5 pin. Note that the filter selection differs between the ADC input path and the DAC output path. See Section 4.7 for more details of the digital filters.

The filter selection for the ADC input path is defined in Table 4-4.

Table 4-4. Hardware Control—ADC Input Digital Filter Selection

Pin Name	Pin Configuration		ADC Decimation Filter [1]	High-Pass Filter (HPF)
CONFIG5	Pull-up to VDD_A	0 Ω	Minimum phase, slow roll-off	Bypass
		4.7 kΩ	Minimum phase, fast roll-off	Bypass
		22 kΩ	Linear phase, slow roll-off	Bypass
		100 kΩ	Linear phase, fast roll-off	Bypass
	Pull-down to GND_A	100 kΩ	Linear phase, fast roll-off	Enabled
		22 kΩ	Linear phase, slow roll-off	Enabled
		4.7 kΩ	Minimum phase, fast roll-off	Enabled
		0 Ω	Minimum phase, slow roll-off	Enabled

1. Fast roll-off filters are supported for all sample rates. Slow roll-off filters are not valid for 32 kHz sample rate.

The filter selection for the DAC output path is defined in Table 4-5. Note the filter selection is dependent on the sample rate.

Table 4-5. Hardware Control—DAC Output Digital Filter Selection

Pin Name	Pin Configuration		DAC Interpolation Filter		High-Pass Filter (HPF)
			32–48 kHz Sample Rate [1]	88.2–192 kHz Sample Rate	
CONFIG5	Pull-up to VDD_A	0 Ω	Minimum phase, slow roll-off	Minimum phase, balanced roll-off	Bypass
		4.7 kΩ	Minimum phase, fast roll-off	Minimum phase, fast roll-off	Bypass
		22 kΩ	Linear phase, slow roll-off	Linear phase, balanced roll-off	Bypass
		100 kΩ	Linear phase, fast roll-off	Linear phase, fast roll-off	Bypass
	Pull-down to GND_A	100 kΩ	Linear phase, fast roll-off	Linear phase, fast roll-off	Enabled
		22 kΩ	Linear phase, slow roll-off	Linear phase, balanced roll-off	Enabled
		4.7 kΩ	Minimum phase, fast roll-off	Minimum phase, fast roll-off	Enabled
		0 Ω	Minimum phase, slow roll-off	Minimum phase, balanced roll-off	Enabled

1.Fast roll-off filters are supported for all sample rates. Slow roll-off filters are not valid for 32 kHz sample rate.

In hardware mode, the device configuration is latched when reset is released (either power-on reset or deassertion of the $\overline{\text{RESET}}$ pin). In hardware mode, the configuration cannot be changed while the device is operational. To update the device configuration, the $\overline{\text{RESET}}$ pin must be asserted (Logic 0), or the device power cycled, in order to read new settings on the CONFIGx pins.

If software mode is selected (i.e., CONFIG1 has a 0 Ω pull-up to VDD_A), the ASP configuration and digital-filter selection are controlled by register writes via the applicable control interface. Unused CONFIGx pins should be terminated as described in Section 1.3.

Notes: In software mode, the CONFIG2, CONFIG3, and CONFIG4 pins can optionally be used to support the hybrid gain control function (see Section 4.5.4).

In software mode, the CONFIG5 pin is used to select the I²C target address (see Section 4.9). If the SPI control interface is used, it is recommended to connect the CONFIG5 pin to GND.

4.3 Software Configuration

Software control mode is enabled if the CONFIG1 pin is connected to VDD_A. In software control mode, the CS4282P is configured by writing to control registers using the control port.

The control port supports I²C and SPI modes of operation; the applicable mode is detected automatically on the respective interface pins. In I²C mode, the target address is selectable using the CONFIG5 pin. See Section 4.9 for further details of the I²C/SPI control port.

In software control mode, GLOBAL_EN is used as the global control field for enabling/disabling the CS4282P functions. The device should be configured using the applicable control registers before setting GLOBAL_EN.

Notes: The clocking (Section 4.4) and ASP (Section 4.8) control registers are only valid on the rising edge of GLOBAL_EN. Writing to these registers has no effect at any other time. It is recommended to select the disabled state (GLOBAL_EN = 0) before writing to these registers.

See Section 4.6.1 to minimize the CS4282P power consumption when all output paths are disabled.

A reset of the CS4282P can be triggered by writing 0x5A to the SW_RESET field. A software reset disables all functions and sets the control registers to their default states.

4.4 System Clocking

Clocking for the CS4282P is provided from the ASP interface (BCLK) or else using the dedicated MCLK input.

The integrated PLL can be used to generate the internal system clock from the external reference. The MCLK signal can be used as a direct clock source, bypassing the PLL. If BCLK is selected as the clock reference, the PLL is always used and cannot be bypassed.

In ASP Secondary Mode, the FSYNC input is used to control the ADC-sample and DAC-conversion timing, enabling multiple CS4282P devices to operate synchronously in a system. See Section 4.8 for more details of the ASP.

The clocking architecture is illustrated in Fig. 4-1.

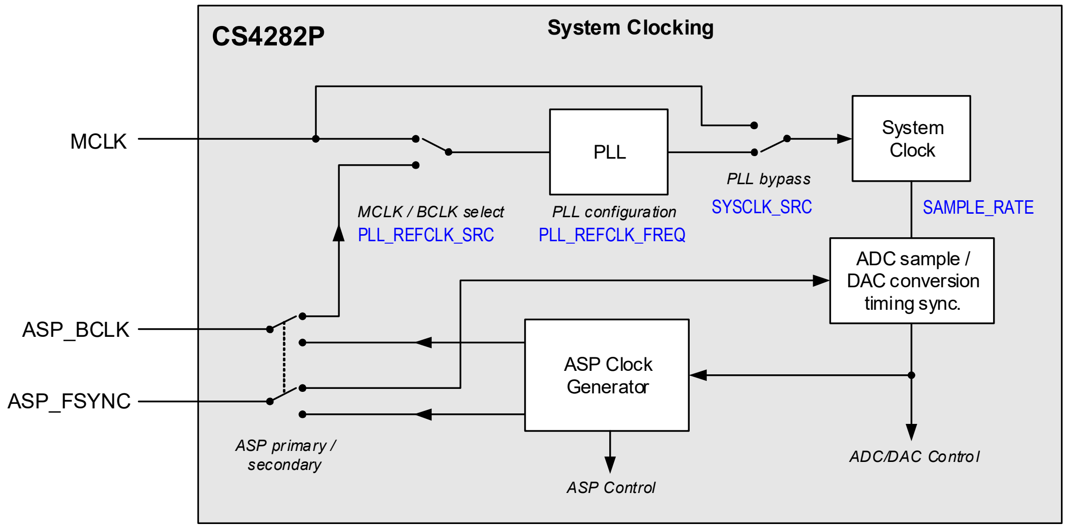


Figure 4-1. System Clocking

4.4.1 Hardware Control Mode

In hardware control mode, the clocking configuration is determined by the CONFIG4 pin (see Section 4.2). Four possible clocking configurations are supported as follows:

- BCLK reference—64 fs, PLL enabled
- MCLK reference—1024 fs(base), PLL bypass
- MCLK reference—256 fs(base), PLL enabled
- MCLK reference—512 fs(base), PLL enabled

The clocking configuration is defined with reference to the sample rate (fs). Note that fs(base) is the *base sample rate*; fs(base) = 48 kHz for 48 kHz-related sample rates, fs(base) = 44.1 kHz for 44.1 kHz-related sample rates.

The sample rate is selected using the CONFIG1 pin as described in Section 4.2. Sample rates 44.1 kHz–192 kHz can be configured, or else the autodetect option (32 kHz–192 kHz) automatically configures the device according to the ASP interface clock signals. Note the autodetect sample-rate option is only valid if the clock reference source is MCLK and the ASP is operating in Secondary Mode (see Section 4.8).

The BCLK 64 fs configuration enables the CS4282P to be clocked from the audio serial port (ASP) operating in Secondary Mode, with no requirement for any other clock reference. Note that, in the BCLK 64 fs clocking configuration, the ASP data format must be either I^2S, left-justified, or TDM (minimum time slots); the TDM (maximum time slots) format is not supported.

The MCLK-referenced configurations use a fixed clock frequency of 12.288 / 24.576 / 49.152 MHz (for 48 kHz-related sample rates), or 11.2896 / 22.5792 / 45.1584 MHz (for 44.1 kHz-related sample rates).

The supported clocking configurations are summarized in Table 4-6.

Table 4-6. System Clock Configuration

Description	PLL Select	Reference Source	Reference Frequency	ASP Operating Conditions [1]
BCLK = 64 fs	Enabled	BCLK	64 × sample rate	Secondary Mode only, I2S, left-justified, or TDM (min slots) formats, sample rates 44.1–192 kHz, sample-rate autodetect not supported.
MCLK = 1024 fs(base)	Bypass	MCLK	49.152 MHz or 45.1584 MHz	Primary or Secondary Mode, I2S, left-justified, or TDM data formats, sample rates 32–192 kHz, sample-rate autodetect supported.
MCLK = 256 fs(base)	Enabled	MCLK	12.288 MHz or 11.2896 MHz	
MCLK = 512 fs(base)	Enabled	MCLK	24.576 MHz or 22.5792 MHz	

1. See Section 4.8 for details of the audio serial port (ASP).

The sample rate must be related to the system clock reference as described in Table 4-7.

Table 4-7. Sample Rate Options

Reference Source	Clocking Configuration	Reference Frequency (MHz)	Sample Rate (kHz)
BCLK	BCLK = 64 fs	2.8224	44.1
		5.6448	88.2
		11.2896	176.4
		3.072	48
		6.144	96
		12.288	192
MCLK	MCLK = 1024 fs(base)	45.1584	44.1, 88.2, 176.4
		49.152	32, 48, 96, 192
	MCLK = 256 fs(base)	11.2896	44.1, 88.2, 176.4
		12.288	32, 48, 96, 192
	MCLK = 512 fs(base)	22.5792	44.1, 88.2, 176.4
		24.576	32, 48, 96, 192

Note that, if MCLK is configured as the clock source (with or without PLL) and the ASP is configured in Secondary Mode, the external clocks (MCLK, BCLK, and FSYNC) must be derived from a common clock source. The clocks must be synchronized, but the phase difference is not important.

4.4.2 Software Control Mode

In software (I2C/SPI) control mode, the clocking configuration is selected using the following control fields:

- The sample rate is configured using SAMPLE_RATE. Sample rates 32 kHz–768 kHz can be configured, or else the autodetect option automatically configures the device according to the ASP interface signals. The sample rate must be related to the system clock reference as described in Table 4-9.

  Note that the sample-rate autodetect option is only valid if all the following conditions are met:
  — Sample rate is 32 kHz–192 kHz
  — The clock reference source is MCLK
  — ASP is operating in Secondary Mode (see Section 4.8).
- The system clock source is selected using SYSCLK_SRC. The clock source can be either MCLK or the output from the PLL. If MCLK is selected (i.e., PLL bypass), the MCLK frequency must be 49.152 MHz (for 48 kHz-related sample rates) or 45.1584 MHz (for 44.1 kHz-related sample rates).
- The input reference to the PLL is selected using PLL_REFCLK_SRC. The reference can be either MCLK or BCLK. Note the BCLK reference is only valid if the ASP is operating in Secondary Mode.
- The frequency of the PLL input reference is configured using PLL_REFCLK_FREQ.

The supported clocking configurations are summarized in Table 4-8.

Table 4-8. System Clock Configuration

SYSCLK_SRC	PLL_REFCLK_SRC	Description	Reference Frequency	Sample Rate Autodetect Supported
0	X	MCLK reference, PLL bypass	49.152 MHz or 45.1584 MHz	Yes
1	1	MCLK reference, PLL enabled	Configured by PLL_REFCLK_FREQ	Yes
1	0	BCLK reference, PLL enabled		No

The sample rate must be related to the system clock reference as described in Table 4-9.

Table 4-9. Sample Rate Options

Reference Frequency (MHz)	PLL_REFCLK_FREQ	Sample Rate (kHz) [1]
2.8224	00	44.1, 88.2, 176.4, 352.8, 705.6
5.6448	01	
11.2896	10	
22.5792	11	
45.1584	See note [2]	
3.072	00	32, 48, 96, 192, 384, 768
6.144	01	
12.288	10	
24.576	11	
49.152	See note [2]	

1. Sample rate is configured using SAMPLE_RATE.
2. Only valid in PLL-bypass configuration. The PLL_REFCLK_FREQ setting is not used.

Note that, if MCLK is configured as the clock source (with or without PLL) and the ASP is configured in Secondary Mode, the external clocks (MCLK, BCLK, and FSYNC) must be derived from a common clock source. The clocks must be synchronized, but the phase difference is not important.

4.5 ADC and Analog Input

The CS4282P supports two analog input channels, each incorporating a high-performance sigma-delta analog-to-digital converter (ADC). Digital volume and mute control is provided on each input channel.

Note that the digital volume and mute controls are supported in software (I^2C/SPI) control mode only. In hardware control mode, all channels are enabled with 0 dB gain.

4.5.1 ADC Path Enable

The analog input and ADC paths are enabled using INx_ADC_EN (where x indicates the channel number 1–2).

Note: Both input paths (1–2) must always be configured in the same state (enabled or disabled). For example, input path 1 should not be enabled without also enabling input path 2.

The polarity of the ADC output can be inverted using INx_INV for the respective channel.

The CS4282P supports selectable impedance on the input pins. The mid-impedance option is configured by default. The input pins can be configured high impedance by setting IN12_HIZ. Note that power consumption is increased in the high-impedance configuration.

4.5.2 Digital Volume and Mute

The ADC signal path incorporates a digital volume control, supporting a gain range of –127.5 dB to 0 dB in 0.5 dB steps. Volume ramping and digital mute is also supported.

The digital volume is configured using INx_VOL for the respective input channel. The digital mute is enabled by setting INx_MUTE.

Writing to the volume or mute fields has no effect on the signal path until a 1 is written to IN_VU. Writing 1 to IN_VU causes the volume and mute settings to be updated on all input paths simultaneously.

When the volume or mute is changed, the gain of the affected signal paths is ramped up or down to the new setting. For increasing gain, the rate is controlled by IN_RAMP_RATE_INC; for decreasing gain, the rate is controlled by IN_RAMP_RATE_DEC.

Note: The IN_RAMP_RATE_INC and IN_RAMP_RATE_DEC fields should not be changed while a volume ramp is in progress.

4.5.3 Input Clip Warning

The CS4282P provides a clip-warning function on the ADC input paths; this can be used to provide a warning of large or clipped signal levels. The clip warning is indicated using latching status bits, and can also be configured as a logic output on a hardware pin.

The clip-warning threshold level is configured using IN_CLIP_THRESH. The selected level applies to all input paths.

If an input signal exceeds the clip-warning threshold, the INx_CLIP_WARN bit is set (where *x* indicates the channel number 1–2). These bits are latching fields which, once set, remain set until a 1 is written to the respective bits. These bits can be polled at any time or in response to the logic output signal being asserted.

The clip-warning status can be configured as a logic output on a hardware pin. This is supported on different pins by setting the applicable control bit shown in Table 4-10.

The logic output is active low, i.e., Logic 0 if the clip-warning threshold is exceeded on any input path. The logic output can be either CMOS driven or open drain; this is selected using CLIP_OP_CFG.

Table 4-10. Clip Warning Output

Pin Name	Power Supply [1]	Output Enable	Notes
CONFIG4	VDD_A	CONFIG4_CLIP_EN	Clip-warning output is not supported if hybrid gain control (see Section 4.5.4) is used.
CONFIG3	VDD_IO	CONFIG3_CLIP_EN	
CONFIG2	VDD_IO	CONFIG2_CLIP_EN	
SPI_CS	VDD_IO	SPI_CS_CLIP_EN	Clip-warning output is not supported if the SPI control port (see Section 4.9.2) is used.
ASP_DOUT2	VDD_IO	ASP_DOUT2_CLIP_EN	Clip-warning output is not supported if the ASP (see Section 4.8) is configured for 705.6 kHz or 768 kHz sample rate.

1.The digital I/O logic levels for each pin are defined with respect to the applicable power supply. See Table 3-11 for details.

4.5.4 Hybrid Gain Control (HGC)

The CS4282P provides the capability to control an external preamplifier (or PGA) associated with the ADC input path. The combination of internal and external gain can be used to optimize the dynamic range of the signal path across a wide range of signal levels.

In typical applications, separate gain stages are provided for analog and digital control of the signal path. The analog stage provides a coarse gain control; the digital stage enables fine adjustment. The CS4282P enables external (analog) and internal (digital) gain adjustments to be fully synchronized across the combined gain range.

A configurable transient-masking function is integrated with the gain-control circuits; this enables seamless gain adjustment by actively suppressing the switching transients often associated with the analog gain selection.

The external PGA is controlled by the CS4282P using a serial interface implemented on the CONFIG pins as shown in Fig. 4-2. Multiple PGAs can be independently controlled in a daisy-chain configuration.

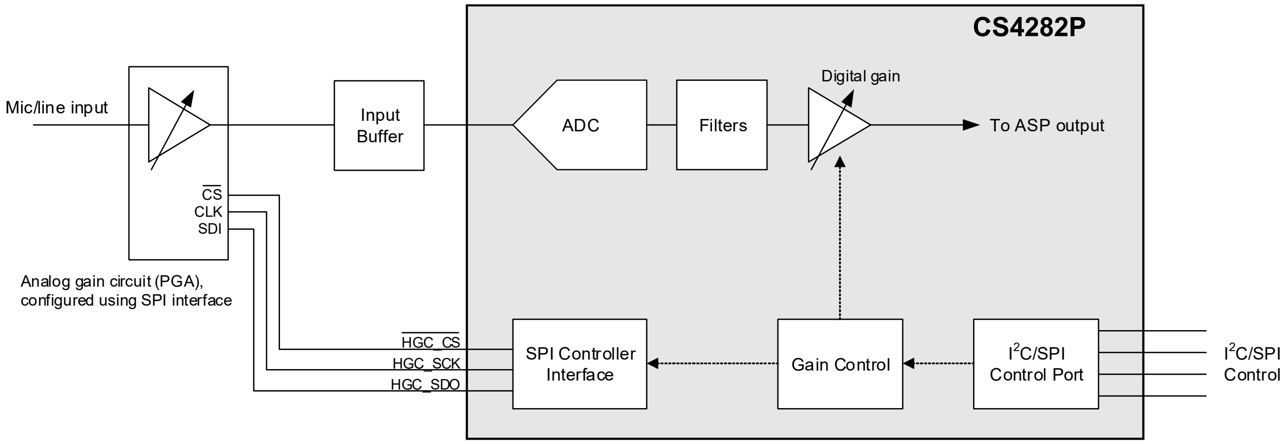


Figure 4-2. Hybrid Gain Control

To configure the signal path, the host processor writes control data to the CS4282P, which then forwards the data to the external PGAs using the serial interface. Zero-cross detection is used to synchronize the PGA configuration with the input signal and with the CS4282P digital volume control, ensuring seamless operation across the combined gain range.

Volume ramping is supported on the internal digital volume (see Section 4.5.2); the volume ramp is coordinated with the external PGA control, enabling smooth transitions across the full range of the internal and external gain selections.

The SPI controller interface can also be used to control auxiliary functions associated with the analog input path (e.g., high-pass filter, pad, or phantom power) using a port expander or similar external IC.

Additional guidance on configuring the HGC function is available in App Note AN0596.

4.5.4.1 SPI Controller Interface Configuration

The SPI controller interface is supported using the CONFIG2, CONFIG3, and CONFIG4 pins, which must be configured for the SPI function if required. The SPI function is enabled using HGC_SPI_EN. The interface comprises three connections as follows:

- CONFIG2/HGC_SCK = Clock output
- CONFIG3/HGC_SDO = Data output
- CONFIG4/$\overline{\text{HGC\_CS}}$ = Chip select ($\overline{\text{CS}}$), active low

Note: The SPI controller connections are powered by VDD_IO. See Table 3-11 for digital I/O levels.

The CS4282P configures the analog gain circuits using a bit pattern which is transmitted to each of the connected devices in a daisy-chain manner. The bit pattern is shifted through each of the connected devices, allowing each device to be individually controlled via a shared data interface.

The SPI interface is fully configurable and flexible to support a wide variety of external gain-control implementations. The SPI data definition is not fixed on the CS4282P; the SPI data can be configured to support whatever bit patterns are required in the specific application.

The number of bits associated with each connected device is configured using the CHx_BIT_PATT_LENGTH field for the respective audio channel. This field should be set to 0 for any audio channel where there is no associated device to be controlled.

A maximum of two auxiliary devices can also be controlled (e.g., for high-pass filter, pad, or phantom-power selection). The number of bits associated with the auxiliary devices is configured using the respective AUXx_BIT_PATT_LENGTH field. This field should be set to 0 if there is no associated device to be controlled.

Typical connections are shown in Fig. 4-3. Note the CS4282P transmits the bit patterns in the sequence AUX2, AUX1, CH2, CH1. The daisy-chain wiring of the external devices must be in the order shown in Fig. 4-3, to ensure each device is configured with its corresponding bit pattern.

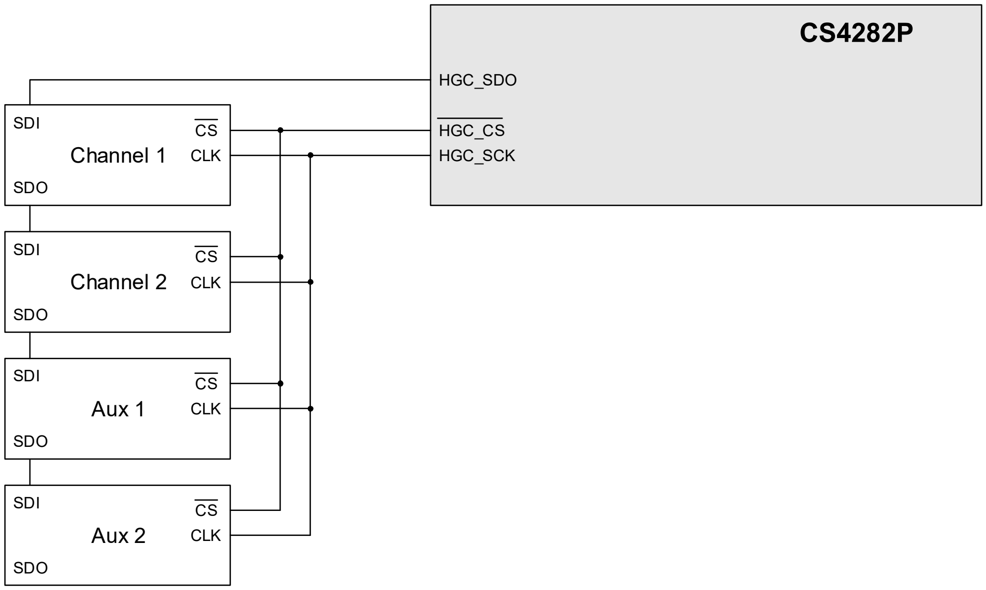


Figure 4-3. Hybrid Gain Interface Connections

The SPI controller is configurable to support different timing and signal-polarity options. The CPOL bit controls the polarity of the clock output; the CPHA bit controls which phase of the clock cycle the data output is valid. See Table 3-17 for timing specifications.

The SPI clock rate is derived as an integer division of the system clock. The SPI clock rate is configured using SCK_DIV, supporting divisors of 24.576 MHz (for 48 kHz-related sample rates), or 22.5792 MHz (for 44.1 kHz-related sample rates). The fastest SPI clock is 12.288 MHz or 11.2896 MHz, depending on sample rate. Slower clock rates can be used to ensure correct timing of the bus signals in applications where a large load capacitance is connected to the SPI outputs.

The minimum idle period between SPI transactions is configured using CS_IDLE_DUR. The delay between the falling $\overline{CS}$ edge and the first SCK edge is configured using CS_FALL_DELAY. The minimum delay between the last SCK edge and the rising $\overline{CS}$ edge is configured using CS_RISE_DELAY.

Note that, in normal operation, the timing of the rising $\overline{CS}$ edge is controlled automatically by the zero-cross detection; the CS_RISE_DELAY field determines the minimum delay.

4.5.4.2 Gain Control Optimization

The CS4282P provides tunable parameters to minimize any audible artifacts when changing the gain configuration.

After a bit pattern has been clocked out to configure the analog gain circuits, the CS4282P waits for a zero-cross detection in the affected audio channel before completing the SPI transaction by deasserting the $\overline{CS}$ signal. This ensures the gain change is aligned with the zero crossing, on the assumption that deasserting the $\overline{CS}$ (Logic 1) causes the new gain setting to be applied immediately in the external circuit. A timeout for zero-cross detection is configured using ZC_TIMEOUT.

The digital gain for each signal path is controlled internally to the CS4282P. After the analog gain is updated, a delay is applied before updating the digital gain. The delay is used to account for the time difference between the analog gain being updated and the change in signal level reaching the gain-control block. The delay, configured using DIG_VOL_DELAY, is used to align the analog and digital gain updates in the audio stream.

The DIG_VOL_DELAY field should be set equal to the sum of the external path delay (analog gain circuit + input buffer) and the ADC filter group delay. The ADC filter characteristics are specified in Table 3-6. The combined delay should be rounded down for the purposes of selecting the nearest DIG_VOL_DELAY option.

A transient-masking function is also available; this is enabled using TM_EN. If enabled, the CS4282P repeats one audio sample for the duration of the transient period, masking the artifact arising from the gain change.

The TM_DELAY field defines the time from the analog gain update to the onset of the transient masking. The duration of the masking is configured using TM_HOLD_TIME.

Transient masking is most effective on low-amplitude signals and is not recommended for larger signals. The CS4282P incorporates a level detector to selectively determine whether the masking should be applied. The transient-masking level detector is enabled on each audio channel using the respective CHx_TM_LD_EN bit. The level detector calculates the signal level using an exponential moving average (EMA) function; the time constant is configurable using TM_LD_TIME.

If the level detector is enabled, the threshold for transient masking is configured using TM_LD_THRESH—masking is applied if the signal level is below the threshold. If the level detector is disabled, transient masking is applied regardless of the signal level.

4.5.4.3 Audio Channel Gain Control

The host processor configures the analog and digital gain for each audio channel by writing to the respective CHx_ANA_VOL and CHx_DIG_VOL fields. The host also writes the CHx_BIT_PATT fields to provide the bit pattern to configure the external device for the required analog gain.

Note: The bit pattern is a maximum of 32 bits (the size is configured using CHx_BIT_PATT_LENGTH). If the bit pattern is 16 bits or less, it is stored in the CHx_BIT_PATT_1 field. The MSB represents the first-transmitted bit of the pattern; one or more of the LSBs may be unused, depending on the size of the bit pattern. If the bit pattern is more than 16 bits, the remaining bits are stored in CHx_BIT_PATT_0.

The analog and digital gain settings do not become effective immediately on updating the control fields. Writing 1 to CHx_UPDATE indicates the settings for the respective audio channel have been updated and are ready to be applied; the CS4282P services each updated channel in turn and applies the respective gain settings at the earliest opportunity. Note that the exact timing varies, dependent on the zero-cross detection for each affected channel.

The BUSY_STS bit, if set, indicates that gain updates are pending for one or more audio channels (i.e., gain settings have been written to the CS4282P, but not yet applied to the respective audio paths). The bit is cleared automatically when all updates have been applied to the respective channels.

Note that the gain settings and bit patterns for each audio channel can be written at any time, regardless of whether an earlier update is currently pending for that channel.

If an audio channel is enabled, but does not have any associated SPI-controlled external gain circuit, the analog gain and digital gain for the respective channel must be maintained at 0 dB (default).

For efficiency of the host-processor interactions, the CHx_BIT_PATT, CHx_ANA_VOL, and CHx_DIG_VOL fields can be written as a contiguous block (i.e., one auto-incrementing I²C/SPI write operation). The CHx_UPDATE bit can be set in the same I²C/SPI operation as writing to the corresponding CHx_DIG_VOL.

Note: If CHx_UPDATE is written 0 when updating the volume/bit-pattern fields, the settings are latched internally but the updates are not applied to the audio path and do not cause the BUSY_STS bit to be set. Writing 0 to CHx_UPDATE is used in the initialization steps described in Section 4.5.4.6. The hybrid gain control must be initialized as described in Section 4.5.4.6 before writing 1 to any of the CHx_UPDATE bits.

4.5.4.4 Gain Ramping Control

The CS4282P supports independent control of the analog (coarse) and digital (fine) gain stages of the input path. When the digital gain is updated, the gain is ramped up or down to the new value; the ramp rate is configurable as described in Section 4.5.2. When the analog gain is updated, the CS4282P uses the digital gain to provide a ramped response, masking the larger step size of the analog gain.

For example, if the analog gain is increased by 3 dB, the gain step is initially canceled out by decreasing the digital gain by –3 dB. Following this, the digital gain is smoothly ramped up by 3 dB to give the desired overall gain.

Note there is no restriction on whether the analog, digital, or both gains are updated in the same operation—the gain ramping is supported for all combinations.

The gain ramping is illustrated in Fig. 4-4. In the example shown, the analog gain is updated from 0 dB to 3 dB. The digital gain is updated from 2 dB to 1 dB. The digital gain is initially set to –1 dB and then ramped to give a smooth transition from 2 dB to 4 dB in the overall (analog + digital) response.

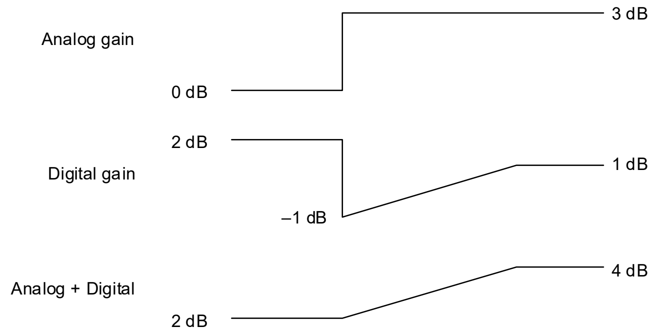


Figure 4-4. Gain Ramping

The gain ramping is configurable using STEP_RAMP_EN. If this bit is set (default), the CS4282P uses a step change in the digital gain to mask the analog gain steps. If this bit is clear, there is no masking of the analog gain steps.

Note: gain ramping is enabled (STEP_RAMP_EN = 1), the volume increasing/decreasing ramp rates must be set to nonzero values. See Section 4.5.2 to configure the volume ramp rates.

4.5.4.5 Auxiliary Device Control

The host processor configures the auxiliary devices by writing to the respective AUXx_BIT_PATT fields. Each field contains the bit pattern to configure the respective external device as required.

Note: The bit pattern is a maximum of 32 bits (the size is configured using AUXx_BIT_PATT_LENGTH). If the bit pattern is 16 bits or less, it is stored in the AUXx_BIT_PATT_1 field. The MSB represents the first-transmitted bit of the pattern; one or more of the LSBs may be unused, depending on the size of the bit pattern. If the bit pattern is more than 16 bits, the remaining bits are stored in AUXx_BIT_PATT_0.

If the auxiliary bit patterns are updated, the new settings are latched internally and are not reflected in the SPI data output until a 1 is written to INIT_UPDATE. Note that the host processor must confirm that the gain controller is idle (BUSY_STS = 0) before writing to INIT_UPDATE.

4.5.4.6 Initialization

The hybrid gain controller must be initialized to ensure correct gain-ramping behavior. The host processor should configure the bit patterns, analog gain, and digital gain fields for all channels—writing CHx_UPDATE = 0 for each audio channel—and then write 1 to INIT_UPDATE to transmit the bit patterns and initialize the internal gain-control algorithms. Note that the host processor must confirm that the gain controller is idle (BUSY_STS = 0) before writing to INIT_UPDATE.

Note: There is no zero-cross detection or transient masking when using INIT_UPDATE, so audible artifacts may occur. It is recommended to mute all audio channels (using INx_MUTE) to suppress any unintended transients.

Writing to INIT_UPDATE has no effect if BUSY_STS = 1, indicating that gain updates are pending for one or more audio channels. The host processor can cancel any pending gain updates by writing 1 to ABORT—this can be used to return the controller to the idle state as quickly as possible, in readiness for initializing the system with a new configuration.

If the ABORT bit is written, the CS4282P does not become idle until it has finished applying the updates to the audio channel currently being processed. The host processor must always check the controller is idle (BUSY_STS = 0) before writing to INIT_UPDATE.

Note: Any gain updates that are canceled using the ABORT bit may result in an inconsistency between the register map and the respective internal/external gain settings. The ABORT bit should only be used as part of a control sequence that also uses INIT_UPDATE to apply a new configuration to all channels.

4.5.5 External Components

The analog input channels are supported using external buffer circuits, also incorporating anti-alias filters. A typical buffer circuit is shown in Fig. 2-1; the typical buffer circuit shown produces a full-scale (0 dBFS) output from a 8 V_{RMS} differential input.

Note that other input-buffer circuit topologies are possible, including support for single-ended input signals and the use of single-ended op-amps.

The CS4282P input impedance is configurable as described in Section 4.5.1. The design of the input buffer circuit should be consistent with the applicable input impedance. The buffer circuit shown in Fig. 2-1 supports both of the available input-impedance selections.

4.6 DAC and Analog Output

The CS4282P supports two analog output channels, each incorporating a high-performance sigma-delta digital-to-analog converter (DAC). Digital volume and mute control is provided on each output channel.

Note that the digital volume and mute controls are supported in software (I^2C/SPI) control mode only. In hardware control mode, all channels are enabled with 0 dB gain.

4.6.1 DAC Path Enable

The analog output and DAC paths are enabled using OUTx_DAC_EN (where x indicates the channel number 1–2).

To minimize power consumption when all output paths are disabled, the DAC reference circuit can be disabled by setting DAC_REF_DISABLE. If this bit is set, all output paths are disabled, regardless of the OUTx_DAC_EN bits.

Note: Power consumption is only reduced if the output paths have previously been enabled. Until they are enabled for the first time, the power consumption is already minimized as far as possible.

When the output paths are enabled for the first time after power-up or after the DAC reference has been disabled, the paths do not become active until a startup delay has elapsed. The time delay (1 s default) is applied when the output paths are enabled using DAC_REF_DISABLE, GLOBAL_EN, or OUTx_DAC_EN ; the delay ensures the noise floor of the output path has settled before it becomes active.

The startup delay can be disabled using STARTUP_DELAY_EN. The delay duration is configurable using STARTUP_DELAY_TIME. If the delay is disabled or is shorter than 1 s, an elevated noise floor (~20 dB above specification) may be observed during the settling period.

The polarity of the DAC output can be inverted using OUTx_INV for the respective channel.

4.6.2 Digital Volume and Mute

The DAC signal path incorporates a digital volume control, supporting a gain range of –127.5 dB to 0 dB in 0.5 dB steps. Volume ramping and digital mute is also supported.

The digital volume is configured using OUTx_VOL for the respective output channel. The digital mute is enabled by setting OUTx_MUTE.

Writing to the volume or mute fields has no effect on the signal path until a 1 is written to OUT_VU. Writing 1 to OUT_VU causes the volume and mute settings to be updated on all output paths simultaneously.

When the volume or mute is changed, the gain of the affected signal paths is ramped up or down to the new setting. For increasing gain, the rate is controlled by OUT_RAMP_RATE_INC; for decreasing gain, the rate is controlled by OUT_RAMP_RATE_DEC.

Note: The OUT_RAMP_RATE_INC and OUT_RAMP_RATE_DEC fields should not be changed while a volume ramp is in progress.

4.6.3 External Components

The analog output channels are supported using external buffer circuits, also incorporating anti-alias filters. A typical buffer circuit is shown in Fig. 2-1; the typical buffer circuit shown produces a 2 V_{RMS} differential output from a full-scale (0 dBFS) digital input.

Note that other output-buffer circuit topologies are possible, including support for single-ended output signals.

4.7 Digital Filter Selection

The ADC input path incorporates a decimation filter and a high-pass filter. Four types of filter are supported:

- Fast roll-off, minimum phase
- Fast roll-off, linear phase
- Slow roll-off, minimum phase
- Slow roll-off, linear phase

The DAC output path incorporates an interpolation filter and a high-pass filter. Six types of filter are supported:

- Fast roll-off, minimum phase
- Fast roll-off, linear phase
- Slow roll-off, minimum phase
- Slow roll-off, linear phase
- Balanced roll-off, minimum phase
- Balanced roll-off, linear phase

The phase-response options is characterized as follows:

- The **minimum-phase** filters offer the lowest latency and an impulse response with no pre-ringing, at the expense of potential in-band phase distortion.
- The **linear-phase** filters have no phase distortion, but also higher latency and a symmetric impulse response.

The frequency-response options are characterized as follows:

- The **fast roll-off** filters maximize the audio signal bandwidth (as a function of the selected sample rate). The fast roll-off filters also provide deep stopband attenuation in the DAC output path. The signal bandwidth and stopband attenuation are prioritized over impulse response and group delay. The deep stopband attenuation minimizes out-of-band noise and aliased signal content.
- The **slow roll-off** filters are optimized for impulse response and group delay, with flat passband over the audible range to 20 kHz. The slow roll-off filters provide a more relaxed stopband specification in the DAC output path. The enhanced impulse response may improve perceived sound quality, especially for transient signal content.
- The **balanced roll-off** filters offer a superior impulse response and group delay as compared with the fast roll-off filters, while retaining a flat passband over the audible range to 20 kHz and deep stopband attenuation.

The ADC input path supports all of the noted filter options for all sample rates. For the DAC output path, the supported filter options for different sample rates are indicated in Table 4-11.

Table 4-11. Digital Filter Options (DAC Output Path)

Description	Sample Rate (kHz)										
	32	44.1	48	88.2	96	176.4	192	352.8	384	705.6	768
Fast roll-off, minimum phase	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Fast roll-off, linear phase	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Slow roll-off, minimum phase	—	Yes	Yes	Yes	Yes	Yes	Yes	—	—	—	—
Slow roll-off, linear phase	—	Yes	Yes	Yes	Yes	Yes	Yes	—	—	—	—
Balanced roll-off, minimum phase	—	—	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Balanced roll-off, linear phase	—	—	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

In hardware control mode, the filter selection is determined by the CONFIG5 pin (see Section 4.2). Note that the filter selection differs between the ADC input path and the DAC output path.

In software (I2C/SPI) control mode, the filters are configured separately for the ADC input and DAC output paths:

- The ADC decimation filter is selected using IN_FILTER_SEL; the high-pass filter is enabled using IN_HPF_EN.
- The DAC interpolation filter is selected using OUT_FILTER_SEL; the high-pass filter is enabled using OUT_HPF_EN.

Performance plots showing the characteristics of the decimation and interpolation filters are shown in Section 7.

A deemphasis filter can also be enabled in the DAC output path. The filter provides standard *Red Book* deemphasis, with corner frequencies corresponding to 15 µs/50 µs time constants, as illustrated in Fig. 4-5.

The deemphasis filter is supported for 32 kHz, 44.1 kHz, and 48 kHz sample rates. The filter is enabled using OUT_DEEMPH_EN. If the sample rate is 44.1 kHz or 48 kHz, the applicable rate must be configured using OUT_DEEMPH_FILT_SEL.

Note: The deemphasis filter is not supported for sample rates above 48 kHz; enabling the filter at sample rates higher than 48 kHz has no effect.

The de-emphasis filter response is illustrated in Fig. 4-5.

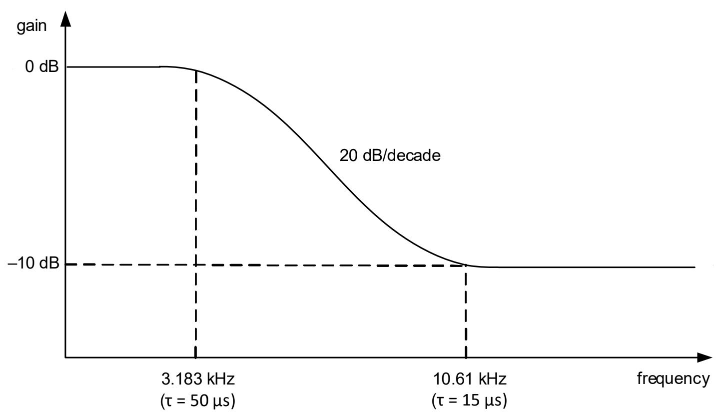


Figure 4-5. Deemphasis Filter Response

4.8 Audio Serial Port (ASP)

The multichannel ASP supports the input/output of digital audio samples to/from the CS4282P. The ASP can be configured as a primary or secondary interface, and supports I2S, left-justified, and TDM data formats. The audio samples can be distributed across two data lines, enabling additional bandwidth and flexibility.

Timing specifications for the ASP are described in Table 3-14. An option is supported to drive the output data (DOUT) on the rising or falling BCLK edge; driving on the rising edge (assuming noninverted BCLK polarity) can be used to support a larger load capacitance by increasing the time between the launching edge from the CS4282P and the sampling edge at the receiving device.

In hardware control mode, the ASP data format is determined by the CONFIGx pins (see Section 4.2). In software (I2C/SPI) control mode, the ASP data format is configured using register fields.

In hardware mode, sample rates 32 kHz–192 kHz are supported. In software mode, the CS4282P supports sample rates 32 kHz–768 kHz.

4.8.1 Primary and Secondary Operation

The ASP interface can operate as a primary or secondary interface. In the primary configuration, the BCLK and FSYNC signals are generated by the CS4282P. In the secondary configuration, the BCLK and FSYNC pins are inputs, allowing another device to drive the respective signals.

In hardware control mode, the ASP is configured as a primary or secondary interface using the CONFIG1 pin (see Section 4.2). In software control mode, the ASP primary/secondary configuration is selected using ASP_PRIMARY.

The ASP operation as a primary or secondary interface is illustrated in Fig. 4-6 and Fig. 4-7.

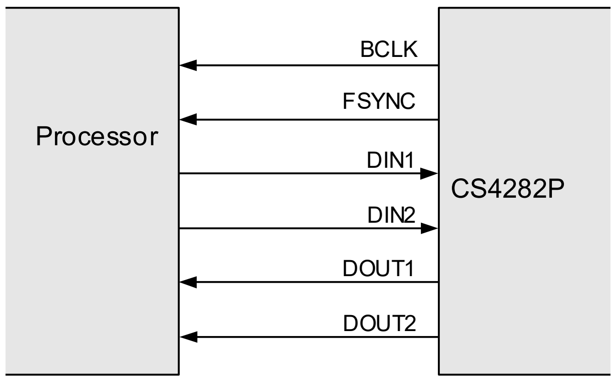


Figure 4-6. Primary Mode

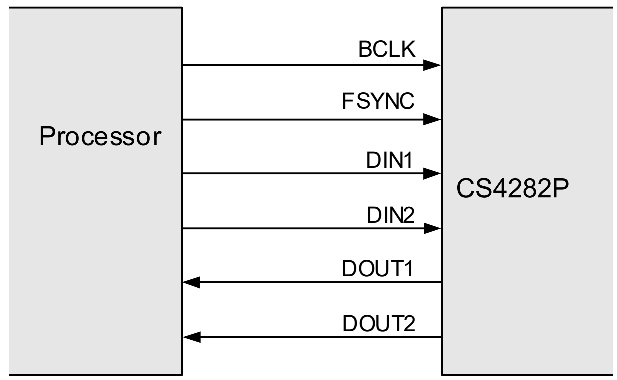


Figure 4-7. Secondary Mode

4.8.2 ASP Data Formats

The ASP interface can be configured to operate in I²S, left-justified, or TDM data formats as illustrated in Fig. 4-8 through Fig. 4-10. The data-bit order is MSB first in each case; data words are encoded in 2's complement (signed, fixed-point) format. Each audio sample is allocated a time slot within the FSYNC frame. Multiple data lines provide capacity to support different audio channels concurrently on different data pins.

- In I²S Mode, the MSB is valid on the second BCLK rising edge following a FSYNC transition. The other bits up to the LSB are valid on each successive BCLK cycle. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

  I²S Mode data format is shown in Fig. 4-8.

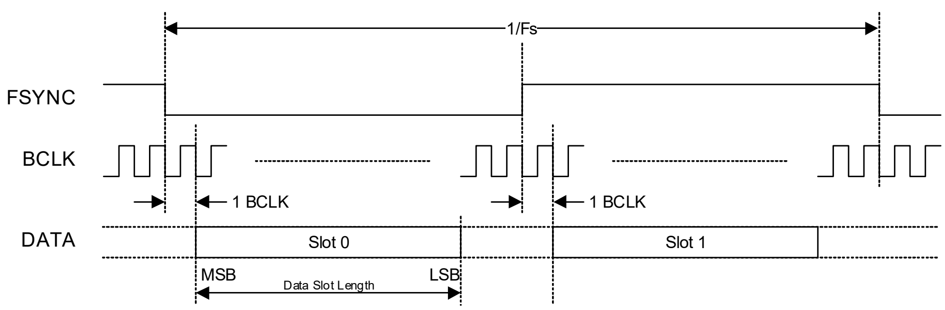


Figure 4-8. I²S Data Format

- In Left-Justified Mode, the MSB is valid on the first BCLK rising edge following a FSYNC transition. The other bits up to the LSB are valid on each successive BCLK cycle. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

  Left-Justified Mode data format is shown in Fig. 4-9.

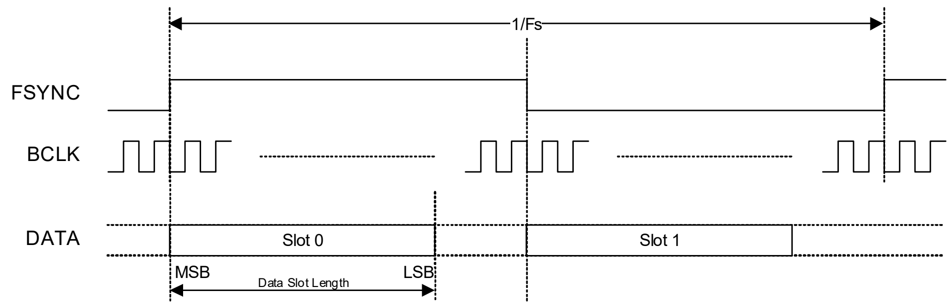


Figure 4-9. Left-Justified Data Format

- In TDM modes, the MSB of the first channel is valid on the second BCLK rising edge following the rising FSYNC edge. Subsequent channels follow immediately after the previous one. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of the last channel data and the start of the next FSYNC frame.

  In Primary Mode, the FSYNC output resembles the frame pulse shown in Fig. 4-10. In Secondary Mode, the FSYNC pulse duration can be anything less than 1/Fs, provided the falling edge of the frame pulse occurs at least one BCLK period before the rising edge of the next frame pulse.

  TDM Mode data format is shown in Fig. 4-10.

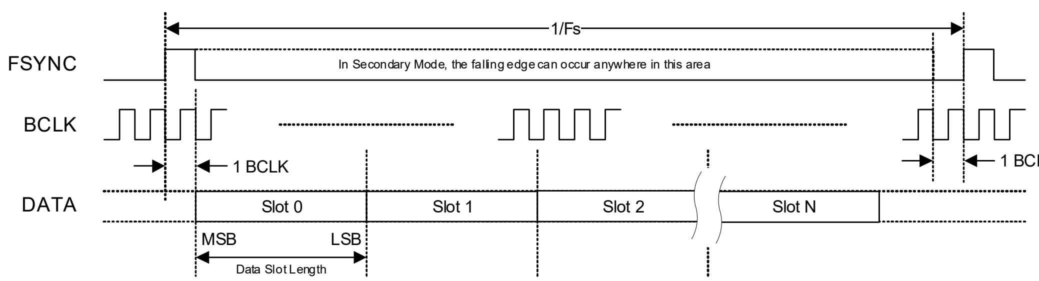


Figure 4-10. TDM Data Format

4.8.3 ASP Configuration

In hardware control mode, the ASP data format is determined by the CONFIG1 and CONFIG2 pins (see Section 4.2).

In software control mode, the ASP data format is configured using SAMPLE_RATE and ASP_FORMAT. If ASP Primary Mode is selected (see Section 4.8.1), the BCLK frequency is configured using ASP_BCLK_FREQ.

In software control mode, the BCLK polarity is selected using ASP_BCLK_INV. The polarity selection is valid in primary and secondary modes, and determines whether the data is valid for sampling on the rising edge or the falling edge.

The BCLK polarity is illustrated in Fig. 4-11 and Fig. 4-12. Note that, in hardware control mode, the BCLK polarity is assumed to be noninverted.

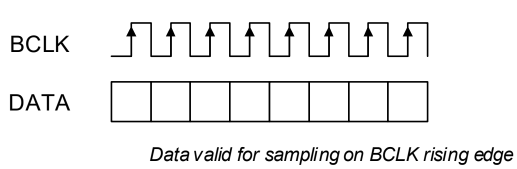


Figure 4-11. Noninverted BCLK

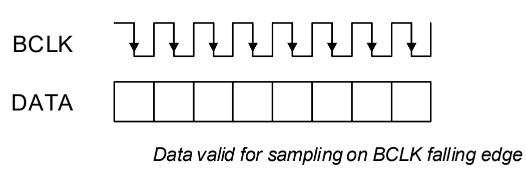


Figure 4-12. Inverted BCLK

In TDM Mode, the two data-format options are supported as follows:

- TDM Mode—minimum time slots. The ASP data format is configured to support the minimum number of time slots necessary for the 2-channel CS4282P input/output. This mode allows the BCLK rate to be as low as possible, equating to a minimum of 32 BCLK cycles per audio sample.
- TDM Mode—maximum time slots. The ASP data format is configured to support the maximum number of time slots for the applicable BCLK rate. The mode is designed for the maximum BCLK rate (22.5792 MHz for 44.1 kHz-related sample rates, or 24.576 MHz for 48 kHz-related sample rates), enabling the maximum possible bandwidth on the ASP data bus to be shared with other devices.

  Note that, for sample rates >192 kHz, the TDM data format is the same regardless of the minimum/maximum time-slot option.

If the ASP is configured for TDM Mode with maximum time slots, the output data (DOUT) can be driven either on the rising or falling BCLK edge. Driving on the rising edge (assuming noninverted BCLK polarity) can be used to support a larger load capacitance by increasing the time between the launching edge from the CS4282P and the sampling edge at the receiving device.

Note that the ASP timing options are dependent on the behavior of the receiving device. It is assumed, for noninverted BCLK, the data is sampled on the rising BCLK edge. Similarly, for inverted BCLK, it is assumed the data is sampled on the falling BCLK edge.

The DOUT drive options for half-cycle and full-cycle mode are described in Table 4-12. In full-cycle mode, the output data is driven on the same BCLK edge as it is sampled (i.e., one full BCLK cycle before the sampling edge).

Table 4-12. TDM Mode (Maximum Time Slots)—DOUT Drive Timing

TDM Mode [1]	BCLK Polarity [2]	DOUT launching (drive) edge	DOUT latching (sampling) edge
Half-cycle	Noninverted	BCLK falling	BCLK rising
	Inverted	BCLK rising	BCLK falling
Full-cycle	Noninverted	BCLK rising	BCLK rising
	Inverted	BCLK falling	BCLK falling

1. The TDM variant is selected using the CONFIG2 pin (in hardware control mode) or ASP_FORMAT (in software control mode).
2. The BCLK polarity is selected using ASP_BCLK_INV in software control mode. In hardware control mode, the polarity is assumed noninverted.

The ASP configuration depends on the sample rate and the selected data format as described in Table 4-13. The input/output data is provided on ASP_DIN1/ASP_DOUT1 in most cases; the ASP_DIN1/ASP_DOUT2 pins are used for 705.6 kHz/768 kHz operation only.

Table 4-13. ASP Data Format

ASP Format [1]	ASP Sample Rate [2,3]	DIN/DOUT pins used	Time slots per frame [4]	BCLK [5,6]
I^{2}S, Left-Justified	32 kHz	1	2	BCLK ≥ 64 fs [7]
	44.1 kHz, 48 kHz	1	2	BCLK ≥ 64 fs
	88.2 kHz, 96 kHz	1	2	BCLK ≥ 64 fs
	176.4 kHz, 192 kHz	1	2	BCLK ≥ 64 fs
	352.8 kHz, 384 kHz	1	2	BCLK = 64 fs
	705.6 kHz, 768 kHz	—	—	—
	Autodetect (32 kHz–192 kHz)	1	2	BCLK ≥ 64 fs
TDM—minimum time slots	32 kHz	1	2	BCLK ≥ 64 fs [7]
	44.1 kHz, 48 kHz	1	2	BCLK ≥ 64 fs
	88.2 kHz, 96 kHz	1	2	BCLK ≥ 64 fs
	176.4 kHz, 192 kHz	1	2	BCLK ≥ 64 fs
	352.8 kHz, 384 kHz	1	2	BCLK = 64 fs
	705.6 kHz, 768 kHz	2	1	BCLK = 32 fs
	Autodetect (32 kHz–192 kHz)	1	2	BCLK ≥ 64 fs
TDM—maximum time slots	32 kHz	1	16	BCLK ≥ 512 fs [7]
	44.1 kHz, 48 kHz	1	16	BCLK = 512 fs
	88.2 kHz, 96 kHz	1	8	BCLK = 256 fs
	176.4 kHz, 192 kHz	1	4	BCLK = 128 fs
	352.8 kHz, 384 kHz	1	2	BCLK = 64 fs
	705.6 kHz, 768 kHz	2	1	BCLK = 32 fs
	Autodetect (32 kHz–192 kHz)	1	4	BCLK ≥ 128 fs

1. The ASP format is selected using the CONFIG2 pin (in hardware control mode) or ASP_FORMAT (in software control mode).
2. The sample rate is selected using the CONFIG1 pin (in hardware control mode) or SAMPLE_RATE (in software control mode).
3. Sample rates 32 kHz–768 kHz supported in software control mode, 32 kHz–192 kHz in hardware control mode.
4. Time slots per frame is the number of data-sample time slots supported on each of the active DIN/DOUT pins.
5. The BCLK rate must be a constant integer multiple of the sample rate (fs).
6. In ASP primary mode (hardware control), the BCLK frequency is the minimum specified rate. In ASP primary mode (software control), the BCLK frequency is configured using ASP_BCLK_FREQ.
7. In ASP primary mode, the specified minimum BCLK frequency for 32 kHz sample rate is not supported. The available options correspond to 96 fs, 192 fs, 384 fs, or 768 fs.

The ASP data format in I^{2}S, Left-Justified, and TDM interface modes as illustrated in Fig. 4-13 through Fig. 4-16. Refer to Table 4-13 for the applicable definition.

- If I^{2}S data format is selected, the ASP supports audio channels 1–2 as shown in Fig. 4-13. The minimum BCLK rate is 64 fs (where fs is the sample rate). A higher BCLK frequency can be used, resulting in unused BCLK cycles between the LSB of one sample and the MSB of the next.

  Note that the input data is provided on ASP_DIN1; the output data is provided on ASP_DOUT1. The ASP_DIN2 and ASP_DOUT2 pins are not used.

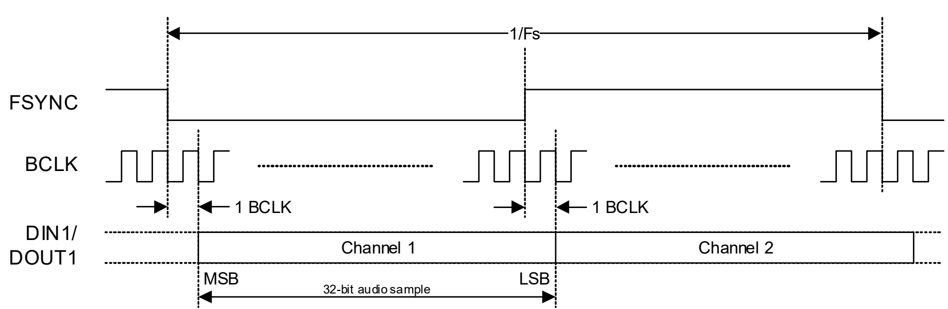


Figure 4-13. I^{2}S Data Format

- If Left-Justified data format is selected, the ASP supports audio channels 1–2 as shown in Fig. 4-14. The minimum BCLK rate is 64 fs (where fs is the sample rate). A higher BCLK frequency can be used, resulting in unused BCLK cycles between the LSB of one sample and the MSB of the next.

  Note that the input data is provided on ASP_DIN1; the output data is provided on ASP_DOUT1. The ASP_DIN2 and ASP_DOUT2 pins are not used

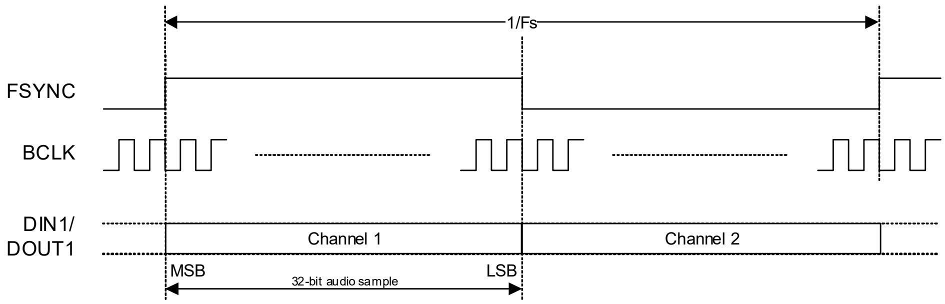


Figure 4-14. Left-Justified Data Format

- In TDM Mode, the FSYNC frame is configured for 1, 2, 4, 8, or 16 slots as specified in Table 4-13.

  In 4-, 8-, and 16-slot modes, the slot assignment for audio channels 1–2 is selected using the CONFIG3 pin (in hardware control mode—see Section 4.2) or else using ASP_TDM_SLOT (in software control mode). In 2-slot modes, the default slot assignment (slots 0–1) should be selected.

  The BCLK rate is related to the sample rate (fs) as described in Table 4-13. Where applicable, the BCLK rate can be higher than the stated minimum, resulting in additional unused BCLK cycles between the last slot in the frame and the start of the next frame.

  The ASP_DOUTn pins are high impedance if the CS4282P is not transmitting data, allowing other devices on the bus to transmit data during any unused time slots.

  In 2-, 4-, 8-, and 16-slot modes, the input data is provided on ASP_DIN1; the output data is provided on ASP_DOUT1. The ASP_DIN2 and ASP_DOUT2 pins are not used.

  The 4-slot TDM format is shown in Fig. 4-15. In the example shown, audio channels 1–2 occupy TDM slots 0–1 respectively.

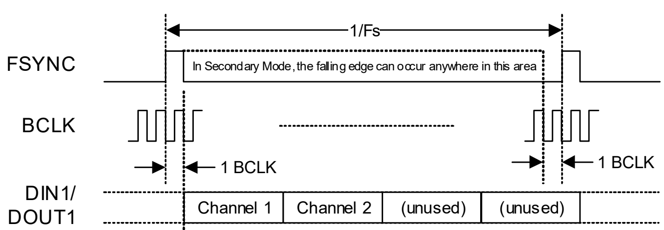


Figure 4-15. TDM Data Format—1 x DIN/DOUT

In 1-slot mode, the input data is provided on ASP_DIN1 and ASP_DIN2; the output data is provided on ASP_DOUT1 and ASP_DOUT2. Note the 1-slot format is used to support 705.6 kHz and 768 kHz sample rates only.

The 1-slot TDM format is shown in Fig. 4-16.

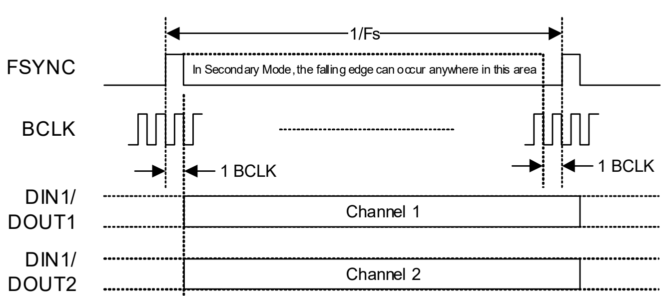


Figure 4-16. TDM Data Format—2 x DIN/DOUT

4.9 I2C/SPI Control Port

The CS4282P incorporates a control port, supporting I2C or SPI modes of operation. In software control mode, the CS4282P is configured by writing to control registers using the control port.

The control port is automatically configured in I2C mode or SPI mode following the first valid I2C/SPI activity detected after power-on or hardware reset.

4.9.1 I2C Control Port

The I2C control port is supported using the I2C_SCL and I2C_SDA pins.

The CS4282P is a target device on the I2C bus—SCL is a clock input, while SDA is a bidirectional data pin. To allow arbitration of multiple targets (and/or multiple controllers) on the same interface, the CS4282P transmits Logic 1 by tristating the SDA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDA line high so that the Logic 1 can be recognized by the controller.

In order to allow many devices to share a single two-wire control bus, every device on the bus has a unique 8-bit device address (this is not the same as the address of each register in the CS4282P). Note that the LSB of the device address is the read/write bit; this bit is set to Logic 1 for read and Logic 0 for write.

The I2C device address is configured using the CONFIG5 pin as described in Table 4-14.

Table 4-14. I2C Address Selection—CONFIG5 pin

Pin Configuration		I2C Address
Pull-up to VDD_A	0 Ω	0x6E (write), 0x6F (read)
	4.7 kΩ	0x6C (write), 0x6D (read)
	22 kΩ	0x6A (write), 0x6B (read)
	100 kΩ	0x68 (write), 0x69 (read)
Pull-down to GND_A	100 kΩ	0x66 (write), 0x67 (read)
	22 kΩ	0x64 (write), 0x65 (read)
	4.7 kΩ	0x62 (write), 0x63 (read)
	0 Ω	0x60 (write), 0x61 (read)

The host device indicates the start of data transfer with a high-to-low transition on SDA while SCL remains high. This indicates that a device address and subsequent address/data bytes follow. The CS4282P responds to the start condition and shifts in the next 8 bits on SDA (8-bit device address, including read/write bit, MSB first). If the device address received matches the device address of the CS4282P, the CS4282P responds by pulling SDA low on the next clock pulse (ACK). If the device address is not recognized or the R/W bit is set incorrectly, the CS4282P returns to the idle condition and waits for a new start condition.

If the device address matches the device address of the CS4282P, the data transfer continues. The controller indicates the end of data transfer with a low-to-high transition on SDA while SCL remains high. After receiving a complete address and data sequence the CS4282P returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e., SDA changes while SCL is high), the device returns to the idle condition.

The I2C interface uses a 16-bit register address and 16-bit data words. The register address must be aligned to a 16-bit word boundary (i.e., the LSB must be 0). Note that the full I2C message protocol also includes a device address, a read/write bit, and other signaling bits (see Fig. 4-17 and Fig. 4-18).

The CS4282P supports the following read and write operations:

- Single write
- Single read
- Multiple write
- Multiple read

Continuous (multiple) read and write modes allow register operations to be scheduled faster than is possible with single register operations. In these modes, the CS4282P automatically increments the register address after each data word. Successive data words can be input/output every two data bytes.

The I2C protocol for a single, 16-bit register write operation is shown in Fig. 4-17.

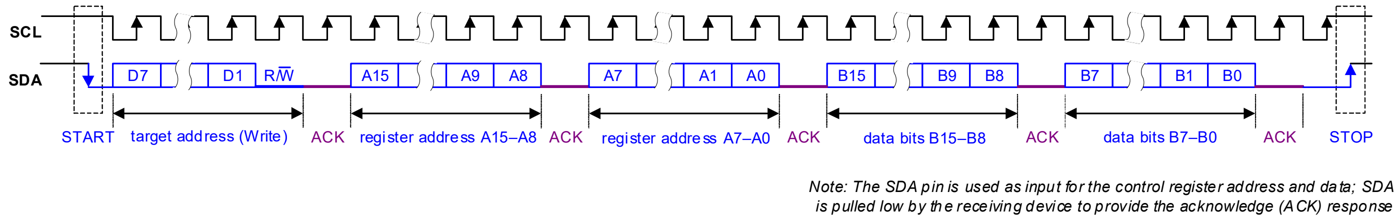


Figure 4-17. Control Interface I2C Register Write

The I2C protocol for a single, 16-bit register read operation is shown in Fig. 4-18.

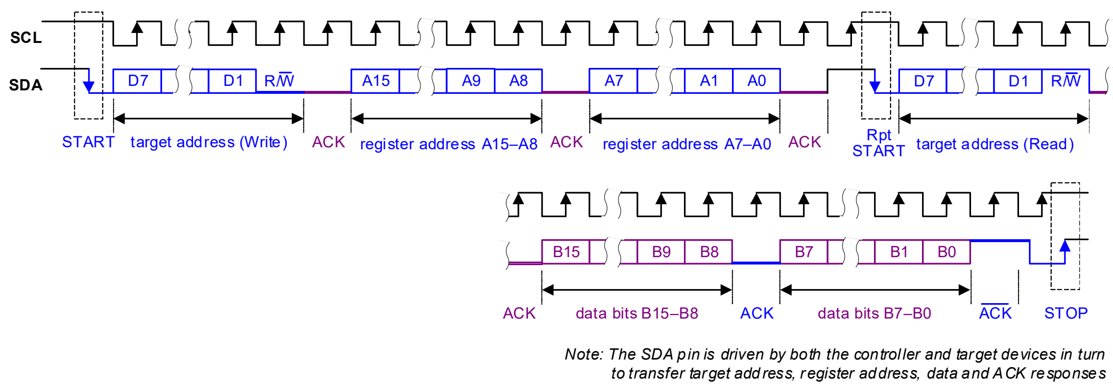


Figure 4-18. Control Interface I2C Register Read

The control interface also supports other register operations; the interface protocol for these operations is shown in Fig. 4-19 through Fig. 4-22. The terminology used in the following figures is detailed in Table 4-15.

Table 4-15. Control Interface (I2C) Terminology

Terminology	Description
S	Start condition
Sr	Repeated start
A	Acknowledge (SDA low)
$\overline{A}$	No Acknowledge (SDA high)
P	Stop condition
R/$\overline{W}$	Read/not Write: 0 = Write, 1 = Read
[White field]	Data flow from bus controller to CS4282P
[Gray field]	Data from CS4282P to bus controller

Fig. 4-19 shows a single register write to a specified address.

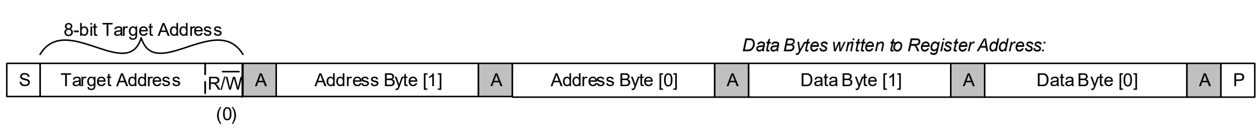


Figure 4-19. Single-Register Write to Specified Address

Fig. 4-20 shows a single register read from a specified address.

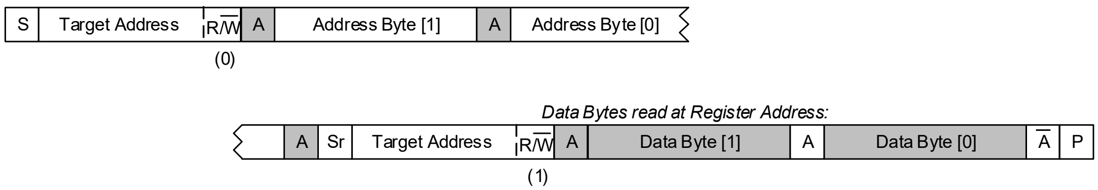


Figure 4-20. Single-Register Read from Specified Address

Fig. 4-21 shows a multiple register write to a specified address.

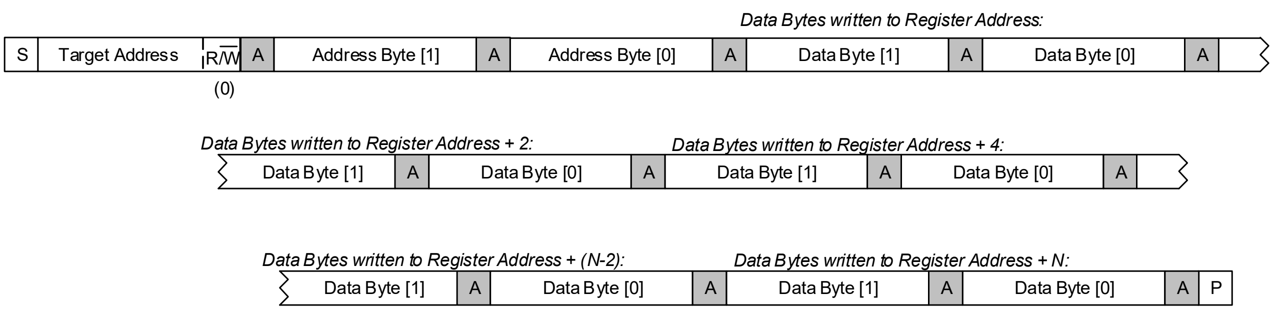


Figure 4-21. Multiple-Register Write to Specified Address

Fig. 4-22 shows a multiple register read from a specified address.

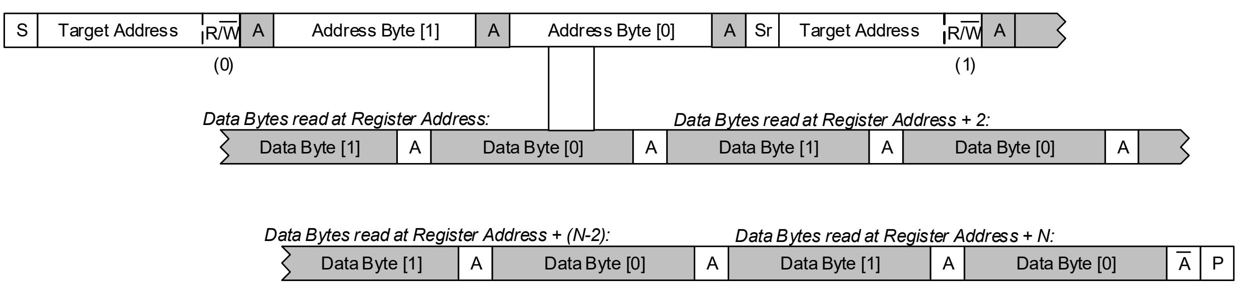


Figure 4-22. Multiple-Register Read from Specified Address

4.9.2 SPI Interface

The SPI interface is supported using the $\overline{\text{SPI\_CS}}$, SPI_SCK, SPI_SDI, and SPI_SDO pins.

The SDI (data-input) pin supports the following behavior:

- In write operations (R/$\overline{\text{W}}$ = 0), the SDI pin input is driven by the controlling device.
- In read operations (R/$\overline{\text{W}}$ = 1), the SDI pin is ignored following receipt of the valid register address.

The SDO (data-output) pin supports the following behavior:

- If $\overline{\text{CS}}$ is asserted (Logic 0), the SDO output is actively driven when outputting data and is high impedance at other times. If $\overline{\text{CS}}$ is not asserted, the SDO output is high impedance.
- The high-impedance state of the SDO output allows the pin to be shared with other peripheral devices.
- The output (SDO) data bit is available to the host device at the rising edge of SCK. See Table 3-16 for timing information.

The SPI interface uses a 15-bit register address and 16-bit data words. Note that the full SPI message protocol also includes a read/write bit and a 16-bit padding phase (see Fig. 4-23 and Fig. 4-24).

Continuous read and write modes enable multiple register operations to be scheduled faster than is possible with single register operations. In these modes, the CS4282P automatically increments the register address at the end of each data word, for as long as $\overline{SS}$ is held low and SCK is toggled. Successive data words can be input/output every 16 clock cycles.

The SPI protocol is shown in Fig. 4-23 and Fig. 4-24.

Fig. 4-23 shows a single register write to a specified address.

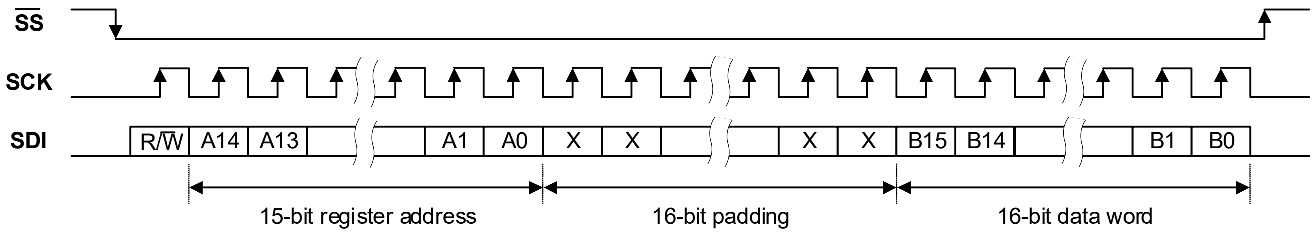


Figure 4-23. Control Interface SPI Register Write

Fig. 4-24 shows a single register read from a specified address.

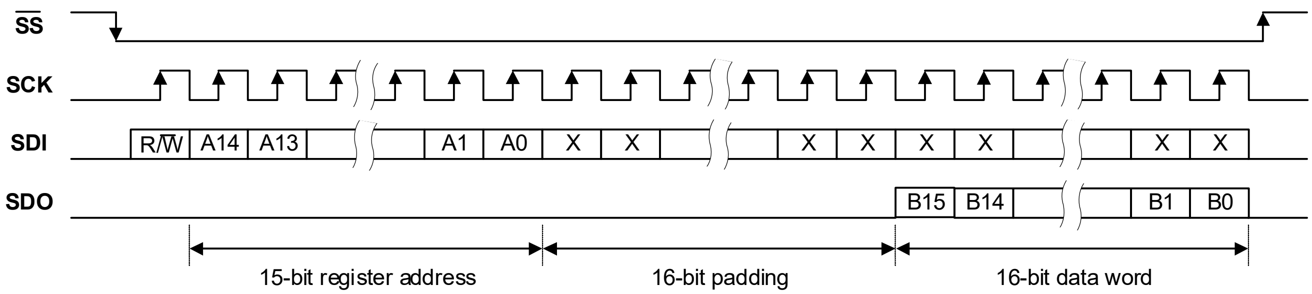


Figure 4-24. Control Interface SPI Register Read

Fig. 4-25 shows a multiple register write to a specified address.

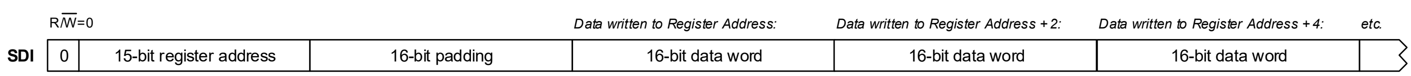


Figure 4-25. Multiple-Register Write to Specified Address

Fig. 4-26 shows a multiple register read from a specified address.

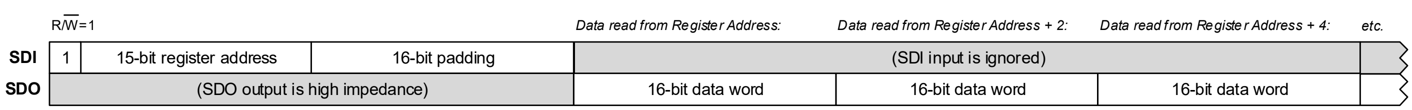


Figure 4-26. Multiple-Register Read from Specified Address

4.10 General-Purpose Output

The CS4282P supports general-purpose outputs on selected digital I/O pins. General-purpose (GP) outputs can be used to provide hardware control signals to other devices.

The general-purpose outputs are multiplexed with other pin functions (e.g., hybrid gain control, I2C/SPI control port, or the audio serial port). Note that care must be taken not to configure a pin for GP output if the shared pin function is required.

Each pin is configured for GP output by setting the respective _FN bit as noted in Table 4-16. If a pin is configured for GP output, the logic output level is selected using the respective _LVL bit.

Table 4-16. General Purpose Output

Pin Name	Power Supply [1]	Pin Function Select	Output Level Select	Notes
CONFIG5	VDD_A	CONFIG5_FN	CONFIG5_LVL	GP output is not supported if the I2C control port (see Section 4.9.1) is used.
CONFIG4/HGC_CS	VDD_A	CONFIG4_FN	CONFIG4_LVL	GP output is not supported if hybrid gain control (see Section 4.5.4) is used.
CONFIG3/HGC_SDO	VDD_IO	CONFIG3_FN	CONFIG3_LVL	
CONFIG2/HGC_SCK	VDD_IO	CONFIG2_FN	CONFIG2_LVL	
SPI_SCK	VDD_IO	SPI_SCK_FN	SPI_SCK_LVL	GP output is not supported if the SPI control port (see Section 4.9.2) is used.
SPI_CS	VDD_IO	SPI_CS_FN	SPI_CS_LVL	
ASP_DIN2	VDD_IO	ASP_DIN2_FN	ASP_DIN2_LVL	GP output is not supported if the ASP (see Section 4.8) is configured for 705.6 kHz or 768 kHz sample rate.
ASP_DOUT2	VDD_IO	ASP_DOUT2_FN	ASP_DOUT2_LVL	

1. The digital I/O logic levels for each pin are defined with respect to the applicable power supply. See Table 3-11 for details.

4.11 Device ID

The device ID, and other associated data, can be read from the control fields listed in Table 4-17.

Table 4-17. Device ID

Label	Description
DEVID	Device ID
AREVID	All-layer device revision
MTLREVID	Metal-layer device revision

5 Register Quick Reference

This section gives an overview of the control port registers. Refer to the following bit definition tables for bit assignment information.

This register view is for the CS4282P.

- The register field default values are established upon the deassertion of the $\overline{\text{RESET}}$ pin or following soft reset.
- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 16 bits wide, and only word transactions are allowed.
- All visible fields are read/write except where indicated with the following shading:

Read/write access — Read-only access — Write-only access

Table 5-1. Block Base Addresses

Base Address	Block Name	Register Quick Reference	Register Description Reference
0x0000 0000	**DEVID**	Section 5.1	Section 6.1
0x0000 0040	**CONFIG**	Section 5.2	Section 6.2
0x0000 0080	**INPUT_PATH**	Section 5.3	Section 6.3
0x0000 00C0	**OUTPUT_PATH**	Section 5.4	Section 6.4
0x0000 2000	**HGC**	Section 5.5	Section 6.5
0x0000 3D00	**PIN_CONFIG**	Section 5.6	Section 6.6
0x0000 3E00	**CLIP_DETECT**	Section 5.7	Section 6.7

5.1 DEVID

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 0000	DEVID	DEVID															
p. 48		0	1	0	0	0	0	1	0	1	0	0	0	0	0	1	0
0x0000 0004	REVID	—								AREVID				MTLREVID			
p. 48		0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0
0x0000 0022	SW_RESET	SW_RESET								—							
p. 48		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

5.2 CONFIG

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 0040	CLK_CFG_0	—			SYSCLK_SRC	—						PLL_REFCLK_FREQ		—			PLL_REFCLK_SRC
p. 49		0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0
0x0000 0042	CLK_CFG_1	—													SAMPLE_RATE		
p. 49		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0x0000 0044	CHIP_ENABLE	—															GLOBAL_EN
p. 49		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0048	ASP_CFG	—									ASP_BCLK_INV	ASP_PRIMARY	—			ASP_BCLK_FREQ	
p. 50		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0050	SIGNAL_PATH_CFG	—						ASP_CH_REVERSE	—			ASP_TDM_SLOT			ASP_FORMAT		
p. 50		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

5.3 INPUT_PATH

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 0080	IN_ENABLES	—														IN2_ ADC_EN	IN1_ ADC_EN
p. 51		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0082	IN_RAMP_SUM	—				IN_CLIP_THRESH				—	IN_RAMP_RATE_DEC			—	IN_RAMP_RATE_INC		
p. 51		0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0
0x0000 0086	IN_FILTER	—			IN_HPF_ EN	—		IN_FILTER_SEL		—							
p. 51		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0088	IN_HIZ	—															IN12_HIZ
p. 52		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 008A	IN_INV	—														IN2_INV	IN1_INV
p. 52		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0090	IN_VOL_ CTRL1_0	IN1_ MUTE	—							IN1_VOL							
p. 52		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0092	IN_VOL_ CTRL1_1	IN2_ MUTE	—							IN2_VOL							
p. 52		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00A0	IN_VOL_CTRL5	—															IN_VU
p. 53		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

5.4 OUTPUT_PATH

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 00C0	OUT_ENABLES	—														OUT2_ DAC_EN	OUT1_ DAC_EN
p. 53		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00C2	OUT_RAMP_ SUM	—									OUT_RAMP_RATE_DEC			—	OUT_RAMP_RATE_INC		
p. 53		0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0
0x0000 00C4	OUT_DEEMPH	—														OUT_ DEEMPH _FILT_ SEL	OUT_ DEEMPH _EN
p. 53		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00C6	OUT_FILTER	—			OUT_ HPF_EN	—	OUT_FILTER_SEL			—							
p. 54		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00CA	OUT_INV	—														OUT2_ INV	OUT1_ INV
p. 54		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00D0	OUT_VOL_ CTRL1_0	OUT1_ MUTE	—							OUT1_VOL							
p. 54		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00D2	OUT_VOL_ CTRL1_1	OUT2_ MUTE	—							OUT2_VOL							
p. 55		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00E0	OUT_VOL_ CTRL5	—															OUT_VU
p. 55		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 00E4	SHUTDOWN_CTRL	—															DAC_REF_DISABLE
p. 55		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00E6	STARTUP_DELAY	—												STARTUP_DELAY_EN	STARTUP_DELAY_TIME		
p. 55		0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

5.5 HGC

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 2000	CONTROL	—											ABORT	—			INIT_UPDATE
p. 56		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2004	STATUS	—															BUSY_STS
p. 56		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2010	GEN_CONFIG	—											STEP_RAMP_EN	—	ZC_TIMEOUT		
p. 56		0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1
0x0000 2014	PATH_DELAY	TM_DELAY								DIG_VOL_DELAY							
p. 57		0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0
0x0000 2018	TM	TM_HOLD_TIME								—							TM_EN
p. 57		0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
0x0000 201C	TM_LD_0	—														CH2_TM_LD_EN	CH1_TM_LD_EN
p. 57		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
0x0000 201E	TM_LD_1	—			TM_LD_THRESH					—			TM_LD_TIME				
p. 58		0	0	0	0	1	0	0	1	0	0	0	0	1	1	0	0
0x0000 2020	SPI_0	—								SCK_DIV				—		CPHA	CPOL
p. 58		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2022	SPI_1	—				CS_IDLE_DUR				CS_RISE_DELAY				CS_FALL_DELAY			
p. 59		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2030	CH1_CONFIG	—										CH1_BIT_PATT_LENGTH					
p. 59		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2034	CH2_CONFIG	—										CH2_BIT_PATT_LENGTH					
p. 60		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2050	AUX1_CONFIG	—										AUX1_BIT_PATT_LENGTH					
p. 60		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2054	AUX2_CONFIG	—										AUX2_BIT_PATT_LENGTH					
p. 60		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2060	CH1_BIT_PATT_0	CH1_BIT_PATT_0															
p. 60		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2062	CH1_BIT_PATT_1	CH1_BIT_PATT_1															
p. 60		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2064	CH1_VOL_0	—					CH1_ANA_VOL										
p. 61		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2066	CH1_VOL_1	CH1_UPDATE	—							CH1_DIG_VOL							
p. 61		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 2068	CH2_BIT_PATT_0	CH2_BIT_PATT_0															
p. 61		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 206A	CH2_BIT_PATT_1	CH2_BIT_PATT_1															
p. 61		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 206C	CH2_VOL_0	—					CH2_ANA_VOL										
p. 62		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 206E	CH2_VOL_1	CH2_UPDATE	—							CH2_DIG_VOL							
p. 62		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 20A0	AUX1_BIT_PATT_0	AUX1_BIT_PATT_0															
p. 62		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 20A2	AUX1_BIT_PATT_1	AUX1_BIT_PATT_1															
p. 62		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 20A4	AUX2_BIT_PATT_0	AUX2_BIT_PATT_0															
p. 63		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 20A6	AUX2_BIT_PATT_1	AUX2_BIT_PATT_1															
p. 63		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

5.6 PIN_CONFIG

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 3D1C	PAD_CLIP	CLIP_OP_CFG	—						CONFIG4_CLIP_EN	CONFIG3_CLIP_EN	CONFIG2_CLIP_EN	—	SPI_CS_CLIP_EN	ASP_DOUT2_CLIP_EN	—		
p. 63		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 3D20	PAD_HGC_SPI	—															HGC_SPI_EN
p. 64		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 3D24	PAD_FN	—						CONFIG5_FN	CONFIG4_FN	CONFIG3_FN	CONFIG2_FN	SPI_SCK_FN	SPI_CS_FN	ASP_DOUT2_FN	—	ASP_DIN2_FN	—
p. 64		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 3D28	PAD_LVL	—						CONFIG5_LVL	CONFIG4_LVL	CONFIG3_LVL	CONFIG2_LVL	SPI_SCK_LVL	SPI_CS_LVL	ASP_DOUT2_LVL	—	ASP_DIN2_LVL	—
p. 64		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

5.7 CLIP_DETECT

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 3E1C	CLIP_WARN	—													IN2_CLIP_WARN	IN1_CLIP_WARN	—
p. 65		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6 Register Descriptions

This section describes each of the control port registers.

This register view is for the CS4282P.

- The register field default values are established upon the deassertion of the $\overline{\text{RESET}}$ pin or following soft reset.
- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 16 bits wide, and only word transactions are allowed.
- All visible fields are read/write except where indicated with the following shading:

Read/write access   Read-only access   Write-only access

6.1 DEVID

6.1.1 DEVID

Address: 0x0000 0000

RO	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEVID															
Default	0	1	0	0	0	0	1	0	1	0	0	0	0	0	1	0

Bits	Name	Description
15:0	DEVID	This register indicates the Device ID CS4282P. 0x0000–0x4281 = Reserved 0x4282 = CS4282P 0x4283–0xFFFF = Reserved

6.1.2 REVID

Address: 0x0000 0004

RO	15…8	7	6	5	4	3	2	1	0
	—	AREVID				MTLREVID			
Default	0x00	1	0	1	0	0	0	0	0

Bits	Name	Description
15:8	—	Reserved
7:4	AREVID	This field indicates the all-layer device revision. 0x0–0x9 = Reserved 0xA = (Default) Revision Ax 0xB–0xF = Reserved
3:0	MTLREVID	This field indicates the metal-layer device revision. 0x0 = (Default) Revision x0 0x1–0xF = Reserved

6.1.3 SW_RESET

Address: 0x0000 0022

WO	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SW_RESET								—							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	SW_RESET	Software Reset. Writing 0x5A triggers a reset. 0x00 = (Default) No action 0x01–0x59 = Reserved 0x5A = Software reset 0x5B–0xFF = Reserved
7:0	—	Reserved

6.2 CONFIG

6.2.1 CLK_CFG_0

Address: 0x0000 0040

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—			SYSCLK_ SRC	—						PLL_REFCLK_FREQ		—			PLL_ REFCLK_ SRC
Default	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0

Bits	Name	Description
15:13	—	Reserved
12	SYSCLK_SRC	System clock source. If MCLK is selected, the PLL is bypassed. 0 = MCLK 1 = (Default) PLL
11:6	—	Reserved
5:4	PLL_REFCLK_FREQ	PLL reference clock frequency. The selection must match the frequency of the selected input reference. 00 = 3.072/2.8224 MHz 01 = 6.144/5.6448 MHz 10 = 12.288/11.2896 MHz 11 = (Default) 24.576/22.5792 MHz
3:1	—	Reserved
0	PLL_REFCLK_SRC	PLL reference clock source. Note the BCLK reference is only valid in ASP Secondary Mode. 0 = (Default) BCLK 1 = MCLK

6.2.2 CLK_CFG_1

Address: 0x0000 0042

RW	15…8	7	6	5	4	3	2	1	0
	—	—					SAMPLE_RATE		
Default	0x00	0	0	0	0	0	0	0	1

Bits	Name	Description
15:3	—	Reserved
2:0	SAMPLE_RATE	Audio sample frequency. Note the sample rate must be integer-related to the system clock frequency. Auto-detect is only valid if sample rate = 32-192kHz, clock reference = MCLK, and the ASP is in Secondary Mode. 000 = 32 kHz 001 = (Default) 48/44.1 kHz 010 = 96/88.2 kHz 011 = 192/176.4 kHz 100 = 384/356.8 kHz 101 = 768/705.6 kHz 110 = Auto-detect 111 = Reserved

6.2.3 CHIP_ENABLE

Address: 0x0000 0044

RW	15…8	7	6	5	4	3	2	1	0
	—	—							GLOBAL_EN
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	GLOBAL_EN	Global enable. Set to 1 to configure and enable all functions. Clear to 0 to disable. Note the clocking and ASP control registers are only valid on the rising edge of GLOBAL_EN. It is recommended to select the disabled state (GLOBAL_EN=0) before writing to these registers.

6.2.4 ASP_CFG

Address: 0x0000 0048

RW	15…8	7	6	5	4	3	2	1	0
	—	—	ASP_BCLK_INV	ASP_PRIMARY	—			ASP_BCLK_FREQ	
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:7	—	Reserved
6	ASP_BCLK_INV	ASP BCLK polarity. Selects the valid BCLK edge for data sampling. In non-inverted mode, data is valid on BCLK rising edge. DOUT data is driven on BCLK falling edge (TDM half-cycle mode) or rising edge (TDM full-cycle mode). In inverted mode, data is valid on BCLK falling edge. DOUT data is driven on BCLK rising edge (TDM half-cycle mode) or falling edge (TSM full-cycle mode). 0 = (Default) Non-inverted 1 = Inverted
5	ASP_PRIMARY	ASP Primary/Secondary Mode select. In ASP Primary Mode, BCLK and FSYNC are outputs. In ASP Secondary Mode, BCLK and FSYNC are inputs. 0 = (Default) Secondary Mode 1 = Primary Mode
4:2	—	Reserved
1:0	ASP_BCLK_FREQ	ASP BCLK frequency. The BCLK frequency must be high enough to support the required number of data bits at the selected sample rate. Only valid in ASP Primary Mode. Note the BCLK frequency is integer-related to the system clock frequency i.e., multiples of 3.072 MHz for 12.288 / 24.576 MHz system clock, or multiples of 2.8224 MHz for 11.2896 / 22.5792 MHz system clock. 00 = (Default) 3.072/2.8224 MHz 01 = 6.144/5.6448 MHz 10 = 12.288/11.2896 MHz 11 = 24.576/22.5792 MHz

6.2.5 SIGNAL_PATH_CFG

Address: 0x0000 0050

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—						ASP_CH_REVERSE	—			ASP_TDM_SLOT			ASP_FORMAT		
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:10	—	Reserved
9	ASP_CH_REVERSE	ASP channel-ordering reversal. Selects normal- or reverse-order ASP data format. 0 = (Default) Normal 1 = Reverse
8:6	—	Reserved
5:3	ASP_TDM_SLOT	TDM slot select. Configures which TDM slots are used in TDM maximum-time-slots mode. 000 = (Default) Slots 0-1 001 = Slots 2-3 010 = Slots 4-5 011 = Slots 6-7 100 = Slots 8-9 101 = Slots 10-11 110 = Slots 12-13 111 = Slots 14-15
2:0	ASP_FORMAT	ASP data format. Selects how the audio samples are arranged within the FSYNC frame. In TDM Maximum Time Slots Full-Cycle Mode, DOUT is driven on same edge as sampling edge. In TDM Maximum Time Slots Half-Cycle Mode, DOUT is driven on opposite edge to sampling edge. 000 = (Default) I2S Mode 001 = Left-Justified Mode 010–100 = Reserved 101 = TDM Maximum Time Slots Full-Cycle Mode 110 = TDM Maximum Time Slots Half-Cycle Mode 111 = TDM Minimum Time Slots Mode

6.3 INPUT_PATH

6.3.1 IN_ENABLES

Address: 0x0000 0080

RW	15…8	7	6	5	4	3	2	1	0
	—	—						IN2_ADC_EN	IN1_ADC_EN
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:2	—	Reserved
1	IN2_ADC_EN	Channel 2 input enable. Note that Channels 1-2 should always be enabled/disabled as a pair. 0 = (Default) Disabled 1 = Enabled
0	IN1_ADC_EN	Channel 1 input enable. Note that Channels 1-2 should always be enabled/disabled as a pair. 0 = (Default) Disabled 1 = Enabled

6.3.2 IN_RAMP_SUM

Address: 0x0000 0082

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				IN_CLIP_THRESH				—	IN_RAMP_RATE_DEC			—	IN_RAMP_RATE_INC		
Default	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0

Bits	Name	Description
15:12	—	Reserved
11:8	IN_CLIP_THRESH	Input clip-warning threshold 0x0 = (Default) 0.0 dBFS 0x1 = –0.125 dBFS 0x2 = –0.25 dBFS 0x3 = –0.5 dBFS 0x4 = –1.0 dBFS 0x5 = –3.0 dBFS 0x6 = –6.0 dBFS 0x7–0xF = Reserved
7	—	Reserved
6:4	IN_RAMP_RATE_DEC	ADC input volume Decrease Ramp Rate (ms/6 dB), used for gain changes including HGC operations. This field should not be changed while a volume ramp is in progress. 000 = 0 ms 001 = 0.5 ms 010 = (Default) 1 ms 011 = 2 ms 100 = 4 ms 101 = 8 ms 110 = 15 ms 111 = 30 ms
3	—	Reserved
2:0	IN_RAMP_RATE_INC	ADC input volume Increase Ramp Rate (ms/6 dB), used for gain changes including HGC operations. This field should not be changed while a volume ramp is in progress. 000 = 0 ms 001 = 0.5 ms 010 = (Default) 1 ms 011 = 2 ms 100 = 4 ms 101 = 8 ms 110 = 15 ms 111 = 30 ms

6.3.3 IN_FILTER

Address: 0x0000 0086

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—			IN_HPF_EN	—		IN_FILTER_SEL		—							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:13	—	Reserved
12	IN_HPF_EN	High-pass filter enable. 0 = (Default) HPF disabled 1 = HPF enabled
11:10	—	Reserved
9:8	IN_FILTER_SEL	Digital filter select. Configures the decimation filter. 00 = (Default) Minimum phase, Slow roll-off 01 = Minimum phase, Fast roll-off 10 = Linear phase, Slow roll-off 11 = Linear phase, Fast roll-off
7:0	—	Reserved

6.3.4 IN_HIZ

Address: 0x0000 0088

RW	15…8	7	6	5	4	3	2	1	0
	—	—							IN12_HIZ
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	IN12_HIZ	Channel 1-2 input impedance select. 0 = (Default) Mid Impedance 1 = High Impedance

6.3.5 IN_INV

Address: 0x0000 008A

RW	15…8	7	6	5	4	3	2	1	0
	—	—						IN2_INV	IN1_INV
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:2	—	Reserved
1	IN2_INV	Channel 2 ADC invert. 0 = (Default) No inversion 1 = ADC data invert
0	IN1_INV	Channel 1 ADC invert. 0 = (Default) No inversion 1 = ADC data invert

6.3.6 IN_VOL_CTRL1_0

Address: 0x0000 0090

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN1_MUTE	—							IN1_VOL							
Default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN1_MUTE	Channel 1 input mute. 0 = Unmute 1 = (Default) Mute
14:8	—	Reserved
7:0	IN1_VOL	Channel 1 input digital volume, –127.5dB to 0dB in 0.5dB steps. 0x00 = (Default) 0.0 dB 0x01 = –0.5 dB … 0xFF = –127.5 dB

6.3.7 IN_VOL_CTRL1_1

Address: 0x0000 0092

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN2_MUTE	—							IN2_VOL							
Default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN2_MUTE	Channel 2 input mute. 0 = Unmute 1 = (Default) Mute
14:8	—	Reserved
7:0	IN2_VOL	Channel 2 input digital volume, –127.5dB to 0dB in 0.5dB steps. 0x00 = (Default) 0.0 dB 0x01 = –0.5 dB … 0xFF = –127.5 dB

6.3.8 IN_VOL_CTRL5

Address: 0x0000 00A0

WO	15…8	7	6	5	4	3	2	1	0
	—	—							IN_VU
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	IN_VU	Global ADC input volume update trigger 0 = (Default) No action 1 = Write 1 to trigger an update of all input volume/mute registers

6.4 OUTPUT_PATH

6.4.1 OUT_ENABLES

Address: 0x0000 00C0

RW	15…8	7	6	5	4	3	2	1	0
	—	—						OUT2_DAC_EN	OUT1_DAC_EN
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:2	—	Reserved
1	OUT2_DAC_EN	Channel 2 output enable. 0 = (Default) Disabled 1 = Enabled
0	OUT1_DAC_EN	Channel 1 output enable. 0 = (Default) Disabled 1 = Enabled

6.4.2 OUT_RAMP_SUM

Address: 0x0000 00C2

RW	15…8	7	6	5	4	3	2	1	0
	—	—	OUT_RAMP_RATE_DEC			—	OUT_RAMP_RATE_INC		
Default	0x00	0	0	1	0	0	0	1	0

Bits	Name	Description
15:7	—	Reserved
6:4	OUT_RAMP_RATE_DEC	DAC output volume decrease Ramp Rate (ms/6 dB), used for gain changes. This field should not be changed while a volume ramp is in progress. 000 = 0 ms 100 = 4 ms 001 = 0.5 ms 101 = 8 ms 010 = (Default) 1 ms 110 = 15 ms 011 = 2 ms 111 = 30 ms
3	—	Reserved
2:0	OUT_RAMP_RATE_INC	DAC output volume increase Ramp Rate (ms/6 dB), used for gain changes. This field should not be changed while a volume ramp is in progress. 000 = 0 ms 100 = 4 ms 001 = 0.5 ms 101 = 8 ms 010 = (Default) 1 ms 110 = 15 ms 011 = 2 ms 111 = 30 ms

6.4.3 OUT_DEEMPH

Address: 0x0000 00C4

RW	15…8	7	6	5	4	3	2	1	0
	—	—						OUT_DEEMPH_FILT_SEL	OUT_DEEMPH_EN
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:2	—	Reserved

Bits	Name	Description
1	OUT_DEEMPH_ FILT_SEL	Deemphasis filter sample-rate selection. 0 = (Default) 44.1 kHz 1 = 48.0 kHz
0	OUT_DEEMPH_EN	Deemphasis filter enable. 0 = (Default) Deemphasis disabled 1 = Deemphasis enabled

6.4.4 OUT_FILTER

Address: 0x0000 00C6

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—			OUT_ HPF_EN	—	OUT_FILTER_SEL			—							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:13	—	Reserved
12	OUT_HPF_EN	High-pass filter enable. 0 = (Default) HPF disabled 1 = HPF enabled
11	—	Reserved
10:8	OUT_FILTER_SEL	Digital filter select. Configures the interpolation filter. 000 = (Default) Minimum phase, Slow roll-off (44.1k-192k) 001 = Minimum phase, Fast roll-off (32k-48k)/Balanced roll-off (88.2k-768k) 010 = Linear phase, Slow roll-off (44.1k-192k) 011 = Linear phase, Fast roll-off (32k-48k)/Balanced roll-off (88.2k-768k) 100 = Reserved 101 = Minimum phase, Fast roll-off (88.2k-768k) 110 = Reserved 111 = Linear phase, Fast roll-off (88.2k-768k)
7:0	—	Reserved

6.4.5 OUT_INV

Address: 0x0000 00CA

RW	15…8	7	6	5	4	3	2	1	0
	—	—						OUT2_INV	OUT1_INV
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:2	—	Reserved
1	OUT2_INV	Channel 2 DAC invert 0 = (Default) No inversion 1 = DAC data invert
0	OUT1_INV	Channel 1 DAC invert 0 = (Default) No inversion 1 = DAC data invert

6.4.6 OUT_VOL_CTRL1_0

Address: 0x0000 00D0

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUT1_ MUTE	—							OUT1_VOL							
Default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	OUT1_MUTE	DAC output channel 1 mute 0 = Unmute 1 = (Default) Mute
14:8	—	Reserved
7:0	OUT1_VOL	DAC output channel 1 Volume, –127.5dB to 0dB in 0.5dB steps 0x00 = (Default) 0.0 dB 0x01 = –0.5 dB … 0xFF = –127.5 dB

6.4.7 OUT_VOL_CTRL1_1

Address: 0x0000 00D2

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUT2_MUTE	—							OUT2_VOL							
Default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	OUT2_MUTE	DAC output channel 2 mute 0 = Unmute 1 = (Default) Mute
14:8	—	Reserved
7:0	OUT2_VOL	DAC output channel 2 Volume, –127.5dB to 0dB in 0.5dB steps 0x00 = (Default) 0.0 dB 0x01 = –0.5 dB … 0xFF = –127.5 dB

6.4.8 OUT_VOL_CTRL5

Address: 0x0000 00E0

WO	15…8	7	6	5	4	3	2	1	0
	—	—							OUT_VU
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	OUT_VU	Global output volume update trigger 0 = (Default) No action 1 = Write 1 to trigger an update of all output volume/mute registers

6.4.9 SHUTDOWN_CTRL

Address: 0x0000 00E4

RW	15…8	7	6	5	4	3	2	1	0
	—	—							DAC_REF_DISABLE
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	DAC_REF_DISABLE	DAC reference shutdown control. Can be used to minimize power consumption if all output paths are disabled. 0 = (Default) Enable DAC reference 1 = Shutdown DAC reference

6.4.10 STARTUP_DELAY

Address: 0x0000 00E6

RW	15…8	7	6	5	4	3	2	1	0
	—	—				STARTUP_DELAY_EN	STARTUP_DELAY_TIME		
Default	0x00	0	0	0	0	1	1	0	0

Bits	Name	Description
15:4	—	Reserved
3	STARTUP_DELAY_EN	Startup delay enable. Can be used to avoid raised noise floor during DAC reference start-up. 0 = Disabled 1 = (Default) Enabled
2:0	STARTUP_DELAY_TIME	Startup delay time. Can be used to avoid raised noise floor during DAC reference start-up. 000 = 100 ms 001 = 250 ms 010 = 500 ms 011 = 750 ms 100 = (Default) 1 s 101 = 1.25 s 110 = 1.5 s 111 = 2 s

6.5 HGC

6.5.1 CONTROL

Address: 0x0000 2000

WO	15…8	7	6	5	4	3	2	1	0
	—	—			ABORT	—			INIT_UPDATE
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:5	—	Reserved
4	ABORT	Abort gain updates. Write 1 to abort any pending gain updates. Note that any updates already in progress will complete as normal and are not aborted. 0 = (Default) No action 1 = Write 1 to abort gain updates
3:1	—	Reserved
0	INIT_UPDATE	Initialize gain settings. Write 1 to transmit the SPI bit patterns and initialize all gain settings. Note the zero-cross detection is not applied when initializing gain settings. 0 = (Default) No action 1 = Write 1 to initialize gain settings

6.5.2 STATUS

Address: 0x0000 2004

RO	15…8	7	6	5	4	3	2	1	0
	—	—							BUSY_STS
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	BUSY_STS	Busy status. Indicates gain updates are pending for one or more audio channels. 0 = (Default) Idle 1 = Busy

6.5.3 GEN_CONFIG

Address: 0x0000 2010

RW	15…8	7	6	5	4	3	2	1	0
	—	—			STEP_RAMP_EN	—	ZC_TIMEOUT		
Default	0x00	0	0	0	1	0	1	1	1

Bits	Name	Description
15:5	—	Reserved
4	STEP_RAMP_EN	Step ramp enable. Enables the digital gain to be used to compensate for step changes in the analog gain. 0 = Disabled 1 = (Default) Enabled
3	—	Reserved
2:0	ZC_TIMEOUT	Timeout for zero-cross detection. 000 = 0 (OFF) 001–010 = Reserved 011 = 1 ms 100 = 2 ms 101 = 5 ms 110 = 10 ms 111 = (Default) 20 ms

6.5.4 PATH_DELAY

Address: 0x0000 2014

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TM_DELAY								DIG_VOL_DELAY							
Default	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0

Bits	Name	Description
15:8	TM_DELAY	Transient masking delay. Configures the delay from the analog-gain update to the start of the transient-masking period. The delay is defined in audio sample (1/fs) units. 0x00 = 0 samples 0x01 = 1 samples … 0x03 = (Default) 3 samples … 0xFF = 255 samples
7:0	DIG_VOL_DELAY	Digital volume update delay. Configures the delay from the analog-gain update to the digital-volume update. The delay is defined in audio sample (1/fs) units. 0x00 = 3 samples 0x01 = 4 samples … 0x04 = (Default) 7 samples … 0xFF = 258 samples

6.5.5 TM

Address: 0x0000 2018

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TM_HOLD_TIME								—							TM_EN
Default	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	TM_HOLD_TIME	Transient masking hold time. Configures the duration of the transient masking. The delay is defined in audio sample (1/fs) units. 0x00 = 0 samples 0x01 = 1 samples … 0x07 = (Default) 7 samples … 0xFF = 255 samples
7:1	—	Reserved
0	TM_EN	Transient masking enable. 0 = (Default) Disabled 1 = Enabled

6.5.6 TM_LD_0

Address: 0x0000 201C

RW	15…8	7	6	5	4	3	2	1	0
	—	—						CH2_TM_LD_EN	CH1_TM_LD_EN
Default	0x00	0	0	0	0	0	0	1	1

Bits	Name	Description
15:2	—	Reserved
1	CH2_TM_LD_EN	Channel 2 transient masking level-detect enable. 0 = Disabled 1 = (Default) Enabled
0	CH1_TM_LD_EN	Channel 1 transient masking level-detect enable. 0 = Disabled 1 = (Default) Enabled

6.5.7 TM_LD_1

Address: 0x0000 201E

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—			TM_LD_THRESH					—			TM_LD_TIME				
Default	0	0	0	0	1	0	0	1	0	0	0	0	1	1	0	0

Bits	Name	Description
15:13	—	Reserved
12:8	TM_LD_THRESH	Transient masking level-detect threshold. Transient masking is applied if the signal level is below the threshold. Signal levels listed are the approximate RMS level of a sine wave that would be detected as just above the threshold. 0x00–0x02 = Reserved 0x03 = –20 dBFS 0x04 = –26 dBFS 0x05 = –32 dBFS 0x06 = –38 dBFS … 0x09 = (Default) –56 dBFS … 0x0E = –86 dBFS 0x0F = –92 dBFS 0x10 = –98 dBFS 0x11 = –104 dBFS 0x12 = –110 dBFS 0x13 = –116 dBFS 0x14–0x1F = Reserved
7:5	—	Reserved
4:0	TM_LD_TIME	Transient masking level-detect time constant. The time constant is defined in audio sample (1/fs) units. 0x00–0x09 = Reserved 0x0A = 1024 samples 0x0B = 2048 samples 0x0C = (Default) 4096 samples 0x0D = 8192 samples 0x0E = 16384 samples 0x0F = 32768 samples 0x10 = 65536 samples 0x11–0x1F = Reserved

6.5.8 SPI_0

Address: 0x0000 2020

RW	15…8	7	6	5	4	3	2	1	0
	—	SCK_DIV				—		CPHA	CPOL
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	—	Reserved
7:4	SCK_DIV	SPI clock divider. Configures the SPI clock frequency as a division of the system clock. For 48 kHz-related sample rates, the SPI clock is a division of 24.576 MHz. For 44.1 kHz-related sample rates, the SPI clock is a division of 22.5792 MHz. 0x0 = (Default) Divide by 2 0x1 = Divide by 4 0x2 = Divide by 6 0x3 = Divide by 8 0x4 = Divide by 10 0x5 = Divide by 12 0x6 = Divide by 14 0x7 = Divide by 16 0x8 = Divide by 18 0x9 = Divide by 20 0xA = Divide by 22 0xB = Divide by 24 0xC = Divide by 26 0xD = Divide by 28 0xE = Divide by 30 0xF = Divide by 32
3:2	—	Reserved
1	CPHA	SPI clock phase select (CPHA) 0 = (Default) Negative SPI clock phase 1 = Positive SPI clock phase
0	CPOL	SPI clock polarity select (CPOL) 0 = (Default) Negative SPI clock polarity 1 = Positive SPI clock polarity

6.5.9 SPI_1

Address: 0x0000 2022

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				CS_IDLE_DUR				CS_RISE_DELAY				CS_FALL_DELAY			
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:12	—	Reserved
11:8	CS_IDLE_DUR	Minimum idle duration between SPI transactions (from CS rising edge to CS falling edge). The duration is defined in system-clock cycles. For 48 kHz-related sample rates, the system-clock period is 1/24.576 MHz. For 44.1 kHz-related sample rates, the system-clock period is 1/22.5792 MHz. 0x0 = (Default) 32 clock cycles 0x1 = 36 clock cycles 0x2 = 40 clock cycles 0x3 = 44 clock cycles 0x4 = 48 clock cycles 0x5 = 56 clock cycles 0x6 = 64 clock cycles 0x7 = 80 clock cycles 0x8 = 96 clock cycles 0x9 = 128 clock cycles 0xA = 160 clock cycles 0xB = 224 clock cycles 0xC = 288 clock cycles 0xD = 416 clock cycles 0xE = 544 clock cycles 0xF = 800 clock cycles
7:4	CS_RISE_DELAY	Chip Select (CS) rise delay. Configures the minimum time from SCLK active edge to CS rising edge (end of SPI transaction). The delay is defined in system-clock cycles. For 48 kHz-related sample rates, the system-clock period is 1/24.576 MHz. For 44.1 kHz-related sample rates, the system-clock period is 1/22.5792 MHz. 0x0 = (Default) 2 clock cycles 0x1 = 4 clock cycles 0x2 = 6 clock cycles 0x3 = 8 clock cycles 0x4 = 10 clock cycles 0x5 = 12 clock cycles 0x6 = 14 clock cycles 0x7 = 16 clock cycles 0x8 = 18 clock cycles 0x9 = 20 clock cycles 0xA = 22 clock cycles 0xB = 24 clock cycles 0xC = 26 clock cycles 0xD = 28 clock cycles 0xE = 30 clock cycles 0xF = 32 clock cycles
3:0	CS_FALL_DELAY	Chip Select (CS) fall delay. Configures the minimum time from CS falling edge (start of SPI transaction) to the first SCK edge. The delay is defined in system-clock cycles. For 48 kHz-related sample rates, the system-clock period is 1/24.576 MHz. For 44.1 kHz-related sample rates, the system-clock period is 1/22.5792 MHz. The delay is dependent on the SPI clock divider (SCK_DIV) setting – the 'N' variable in the enumeration represents the value of SCK_DIV field (0-15). 0x0 = (Default) 3+N clock cycles 0x1 = 5+N clock cycles 0x2 = 7+N clock cycles 0x3 = 9+N clock cycles 0x4 = 11+N clock cycles 0x5 = 13+N clock cycles 0x6 = 15+N clock cycles 0x7 = 17+N clock cycles 0x8 = 19+N clock cycles 0x9 = 21+N clock cycles 0xA = 23+N clock cycles 0xB = 25+N clock cycles 0xC = 27+N clock cycles 0xD = 29+N clock cycles 0xE = 31+N clock cycles 0xF = 33+N clock cycles

6.5.10 CH1_CONFIG

Address: 0x0000 2030

RW	15…8	7	6	5	4	3	2	1	0
	—	—		CH1_BIT_PATT_LENGTH					
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:6	—	Reserved
5:0	CH1_BIT_PATT_LENGTH	Channel 1 bit-pattern length for SPI gain control 0x00 = (Default) 0 bits (device not present) 0x01 = 1 bits 0x02 = 2 bits … 0x20 = 32 bits 0x21–0x3F = Reserved

6.5.11 CH2_CONFIG

Address: 0x0000 2034

RW	15…8	7	6	5	4	3	2	1	0
	—	—		CH2_BIT_PATT_LENGTH					
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:6	—	Reserved
5:0	CH2_BIT_PATT_LENGTH	Channel 2 bit-pattern length for SPI gain control 0x00 = (Default) 0 bits (device not present) 0x01 = 1 bits 0x02 = 2 bits … 0x20 = 32 bits 0x21–0x3F = Reserved

6.5.12 AUX1_CONFIG

Address: 0x0000 2050

RW	15…8	7	6	5	4	3	2	1	0
	—	—		AUX1_BIT_PATT_LENGTH					
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:6	—	Reserved
5:0	AUX1_BIT_PATT_LENGTH	Auxiliary 1 bit-pattern length for SPI aux control 0x00 = (Default) 0 bits (device not present) 0x01 = 1 bits 0x02 = 2 bits … 0x20 = 32 bits 0x21–0x3F = Reserved

6.5.13 AUX2_CONFIG

Address: 0x0000 2054

RW	15…8	7	6	5	4	3	2	1	0
	—	—		AUX2_BIT_PATT_LENGTH					
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:6	—	Reserved
5:0	AUX2_BIT_PATT_LENGTH	Auxiliary 2 bit-pattern length for SPI aux control 0x00 = (Default) 0 bits (device not present) 0x01 = 1 bits 0x02 = 2 bits … 0x20 = 32 bits 0x21–0x3F = Reserved

6.5.14 CH1_BIT_PATT_0

Address: 0x0000 2060

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_BIT_PATT_0															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	CH1_BIT_PATT_0	Channel 1 SPI bit pattern for external gain control, bits 17-32. Only used if the bit pattern is longer than 16 bits. The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 32 bits, one or more of the LSBs is unused.

6.5.15 CH1_BIT_PATT_1

Address: 0x0000 2062

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_BIT_PATT_1															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	CH1_BIT_PATT_1	Channel 1 SPI bit pattern for external gain control, bits 1-16. The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 16 bits, one or more of the LSBs is unused.

6.5.16 CH1_VOL_0

Address: 0x0000 2064

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—					CH1_ANA_VOL										
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:11	—	Reserved
10:0	CH1_ANA_VOL	Channel 1 analog gain. The selected value must match the analog gain of the associated SPI bit pattern. 0x000 = (Default) 0.000 dB 0x001 = 0.125 dB 0x002 = 0.250 dB … 0x23F = 71.875 dB 0x240–0x5BF = Reserved 0x5C0 = –72.000 dB … 0x7FF = –0.125 dB

6.5.17 CH1_VOL_1

Address: 0x0000 2066

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_UPDATE	—							CH1_DIG_VOL							
Access	WO	—							RW							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	CH1_UPDATE	Channel 1 gain update. Write 1 to apply the Channel 1 gain selection and SPI bit pattern. The gain update is applied at the next scheduling opportunity, zero-cross aligned.
14:8	—	Reserved
7:0	CH1_DIG_VOL	Channel 1 digital gain. 0x00 = (Default) 0.000 dB 0x01 = 0.125 dB 0x02 = 0.250 dB … 0x5F = 11.875 dB 0x60–0x9F = Reserved 0xA0 = –12.000 dB … 0xFF = –0.125 dB

6.5.18 CH2_BIT_PATT_0

Address: 0x0000 2068

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_BIT_PATT_0															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	CH2_BIT_PATT_0	Channel 2 SPI bit pattern for external gain control, bits 17-32. Only used if the bit pattern is longer than 16 bits. The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 32 bits, one or more of the LSBs is unused.

6.5.19 CH2_BIT_PATT_1

Address: 0x0000 206A

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_BIT_PATT_1															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	CH2_BIT_PATT_1	Channel 2 SPI bit pattern for external gain control, bits 1-16. The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 16 bits, one or more of the LSBs is unused.

6.5.20 CH2_VOL_0

Address: 0x0000 206C

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—					CH2_ANA_VOL										
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:11	—	Reserved
10:0	CH2_ANA_VOL	Channel 2 analog gain. The selected value must match the analog gain of the associated SPI bit pattern. 0x000 = (Default) 0.000 dB 0x001 = 0.125 dB 0x002 = 0.250 dB … 0x23F = 71.875 dB 0x240–0x5BF = Reserved 0x5C0 = –72.000 dB … 0x7FF = –0.125 dB

6.5.21 CH2_VOL_1

Address: 0x0000 206E

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_UPDATE	—							CH2_DIG_VOL							
Access	WO	—							RW							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	CH2_UPDATE	Channel 2 gain update. Write 1 to apply the Channel 2 gain selection and SPI bit pattern. The gain update is applied at the next scheduling opportunity, zero-cross aligned.
14:8	—	Reserved
7:0	CH2_DIG_VOL	Channel 2 digital gain. 0x00 = (Default) 0.000 dB 0x01 = 0.125 dB 0x02 = 0.250 dB … 0x5F = 11.875 dB 0x60–0x9F = Reserved 0xA0 = –12.000 dB … 0xFF = –0.125 dB

6.5.22 AUX1_BIT_PATT_0

Address: 0x0000 20A0

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AUX1_BIT_PATT_0															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	AUX1_BIT_PATT_0	Auxiliary 1 SPI bit pattern for external gain control, bits 17-32. Only used if the bit pattern is longer than 16 bits. The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 32 bits, one or more of the LSBs is unused.

6.5.23 AUX1_BIT_PATT_1

Address: 0x0000 20A2

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AUX1_BIT_PATT_1															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	AUX1_BIT_PATT_1	Auxiliary 1 SPI bit pattern for external gain control, bits 1-16. The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 16 bits, one or more of the LSBs is unused.

6.5.24 AUX2_BIT_PATT_0

Address: 0x0000 20A4

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AUX2_BIT_PATT_0															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	AUX2_BIT_PATT_0	Auxiliary 2 SPI bit pattern for external gain control, bits 17-32. Only used if the bit pattern is longer than 16 bits. The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 32 bits, one or more of the LSBs is unused.

6.5.25 AUX2_BIT_PATT_1

Address: 0x0000 20A6

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AUX2_BIT_PATT_1															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	AUX2_BIT_PATT_1	Auxiliary 2 SPI bit pattern for external gain control, bits 1-16. The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 16 bits, one or more of the LSBs is unused.

6.6 PIN_CONFIG

6.6.1 PAD_CLIP

Address: 0x0000 3D1C

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CLIP_OP_CFG	—						CONFIG4_CLIP_EN	CONFIG3_CLIP_EN	CONFIG2_CLIP_EN	—	SPI_CS_CLIP_EN	ASP_DOUT2_CLIP_EN	—		
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	CLIP_OP_CFG	Clip-detect output configuration 0 = (Default) CMOS 1 = Open drain
14:9	—	Reserved
8	CONFIG4_CLIP_EN	CONFIG4 pin function select 0 = (Default) HW config 1 = Clip-detect output
7	CONFIG3_CLIP_EN	CONFIG3 pin function select 0 = (Default) HW config 1 = Clip-detect output
6	CONFIG2_CLIP_EN	CONFIG2 pin function select 0 = (Default) HW config 1 = Clip-detect output
5	—	Reserved
4	SPI_CS_CLIP_EN	SPI_CS pin function select 0 = (Default) SPI_CS 1 = Clip-detect output
3	ASP_DOUT2_CLIP_EN	ASP_DOUT2 pin function select 0 = (Default) ASP_DOUT2 1 = Clip-detect output
2:0	—	Reserved

6.6.2 PAD_HGC_SPI

Address: 0x0000 3D20

RW	15…8	7	6	5	4	3	2	1	0
	—	—							HGC_SPI_EN
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	HGC_SPI_EN	HGC pin function select. Set this bit to enable the HGC function on the CONFIG2, CONFIG3, and CONFIG4 pins 0 = (Default) CONFIG function 1 = HGC function

6.6.3 PAD_FN

Address: 0x0000 3D24

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—						CONFIG5_FN	CONFIG4_FN	CONFIG3_FN	CONFIG2_FN	SPI_SCK_FN	SPI_CS_FN	ASP_DOUT2_FN	—	ASP_DIN2_FN	—
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:10	—	Reserved
9	CONFIG5_FN	CONFIG5 pin function select 0 = (Default) HW config 1 = GP output
8	CONFIG4_FN	CONFIG4 pin function select 0 = (Default) HW config 1 = GP output
7	CONFIG3_FN	CONFIG3 pin function select 0 = (Default) HW config 1 = GP output
6	CONFIG2_FN	CONFIG2 pin function select 0 = (Default) HW config 1 = GP output
5	SPI_SCK_FN	SPI_SCK pin function select 0 = (Default) SPI_SCK 1 = GP output
4	SPI_CS_FN	SPI_CS pin function select 0 = (Default) SPI_CS 1 = GP output
3	ASP_DOUT2_FN	ASP_DOUT2 pin function select 0 = (Default) ASP_DOUT2 1 = GP output
2	—	Reserved
1	ASP_DIN2_FN	ASP_DIN2 pin function select 0 = (Default) ASP_DIN2 1 = GP output
0	—	Reserved

6.6.4 PAD_LVL

Address: 0x0000 3D28

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—						CONFIG5_LVL	CONFIG4_LVL	CONFIG3_LVL	CONFIG2_LVL	SPI_SCK_LVL	SPI_CS_LVL	ASP_DOUT2_LVL	—	ASP_DIN2_LVL	—
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:10	—	Reserved
9	CONFIG5_LVL	CONFIG5 output level. Sets the output level if CONFIG5 is configured as GP output. 0 = (Default) Logic 0 1 = Logic 1

Bits	Name	Description
8	CONFIG4_LVL	CONFIG4 output level. Sets the output level if CONFIG4 is configured as GP output. 0 = (Default) Logic 0 1 = Logic 1
7	CONFIG3_LVL	CONFIG3 output level. Sets the output level if CONFIG3 is configured as GP output. 0 = (Default) Logic 0 1 = Logic 1
6	CONFIG2_LVL	CONFIG2 output level. Sets the output level if CONFIG2 is configured as GP output. 0 = (Default) Logic 0 1 = Logic 1
5	SPI_SCK_LVL	SPI_SCK output level. Sets the output level if SPI_SCK is configured as GP output. 0 = (Default) Logic 0 1 = Logic 1
4	SPI_CS_LVL	SPI_CS output level. Sets the output level if SPI_CS is configured as GP output. 0 = (Default) Logic 0 1 = Logic 1
3	ASP_DOUT2_LVL	ASP_DOUT2 output level. Sets the output level if ASP_DOUT2 is configured as GP output. 0 = (Default) Logic 0 1 = Logic 1
2	—	Reserved
1	ASP_DIN2_LVL	ASP_DIN2 output level. Sets the output level if ASP_DIN2 is configured as GP output. 0 = (Default) Logic 0 1 = Logic 1
0	—	Reserved

6.7 CLIP_DETECT

6.7.1 CLIP_WARN

Address: 0x0000 3E1C

RW	15…8	7	6	5	4	3	2	1	0
	—	—					IN2_CLIP_WARN	IN1_CLIP_WARN	—
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:3	—	Reserved
2	IN2_CLIP_WARN	Channel 2 clip-detect indication. Rising edge triggered. Write 1 to clear. 0 = (Default) Normal 1 = Clip detect
1	IN1_CLIP_WARN	Channel 1 clip-detect indication. Rising edge triggered. Write 1 to clear. 0 = (Default) Normal 1 = Clip detect
0	—	Reserved

7 Performance Plots

7.1 ADC Filter Response

The ADC filter performance is described in this section. Note that the group-delay plots represent the filter only—see Table 3-6 for full-path latency.

ADC Filter Response—Fast Roll-Off, 32 kHz Sample Rate

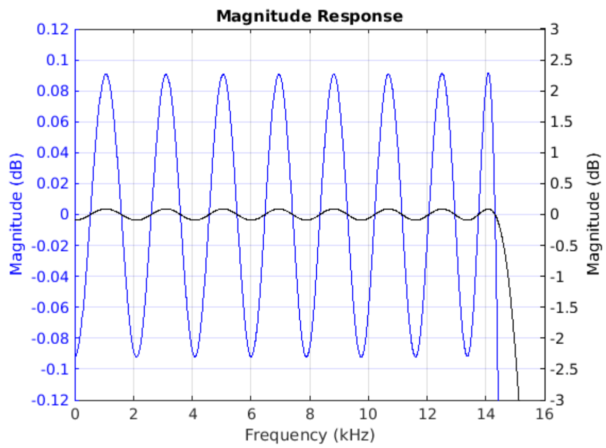


Figure 7-1. Passband Magnitude

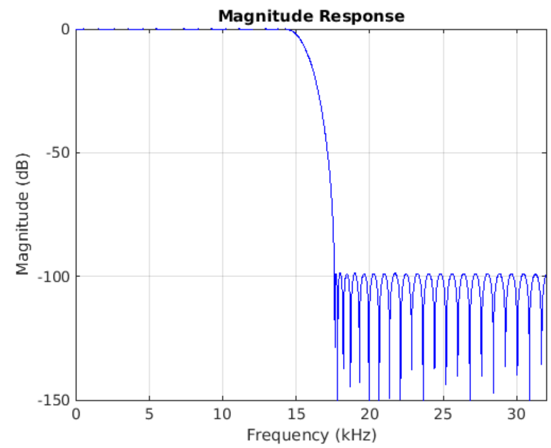


Figure 7-2. Stopband Magnitude

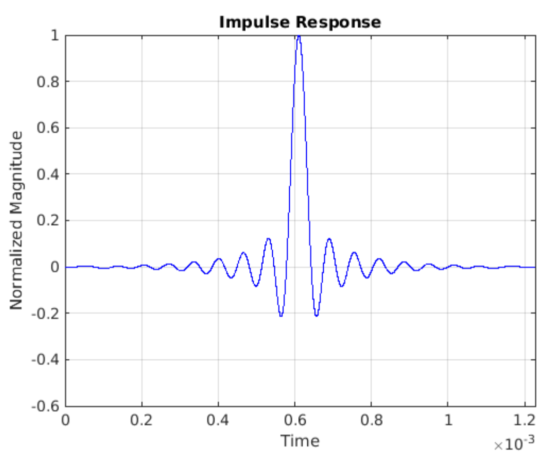


Figure 7-3. Impulse Response—Linear Phase

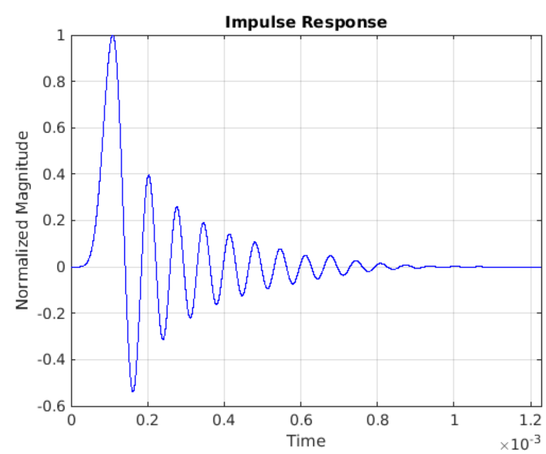


Figure 7-4. Impulse Response—Minimum Phase

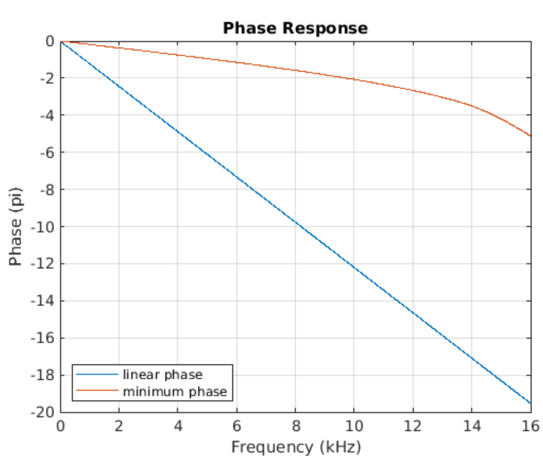


Figure 7-5. Phase vs. Frequency

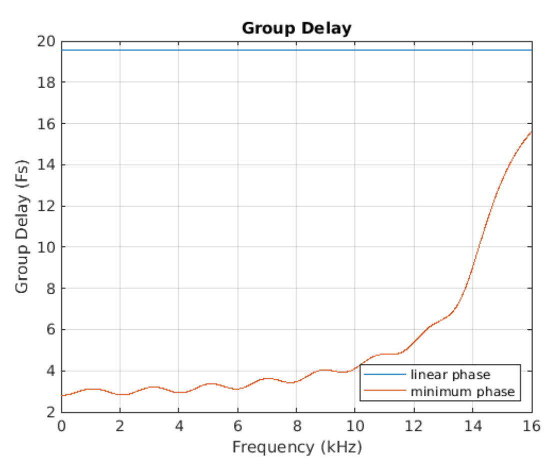


Figure 7-6. Group Delay vs. Frequency

ADC Filter Response—Fast Roll-Off, 48 kHz Sample Rate

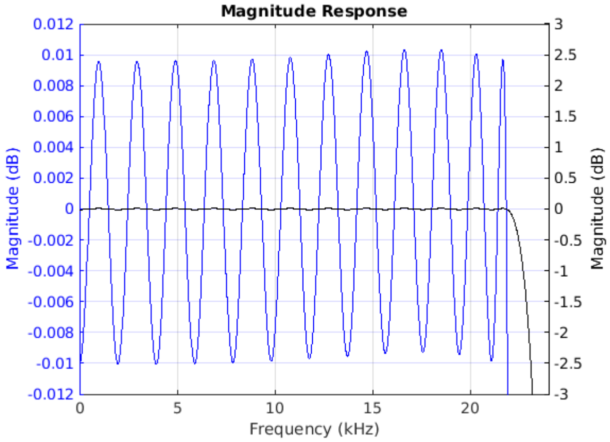


Figure 7-7. Passband Magnitude

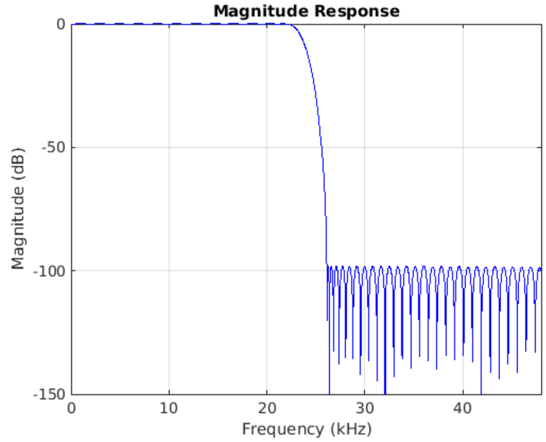


Figure 7-8. Stopband Magnitude

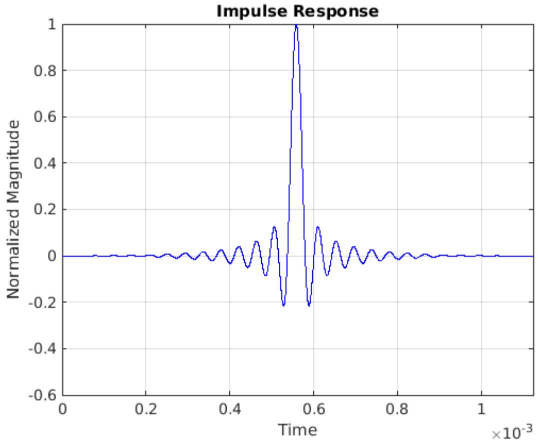


Figure 7-9. Impulse Response—Linear Phase

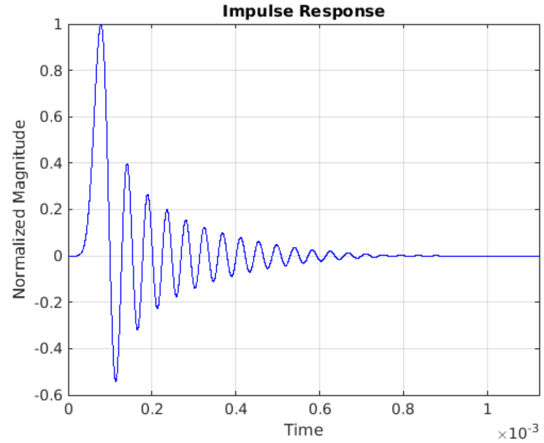


Figure 7-10. Impulse Response—Minimum Phase

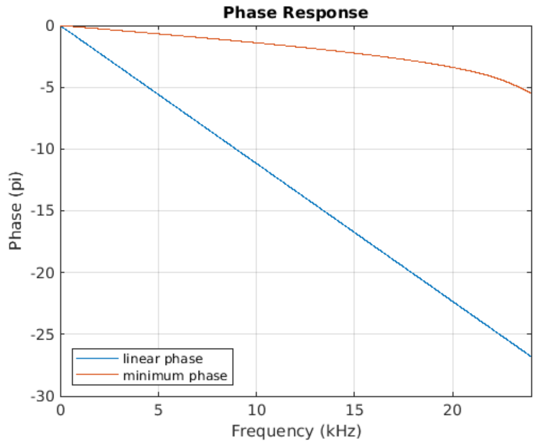


Figure 7-11. Phase vs. Frequency

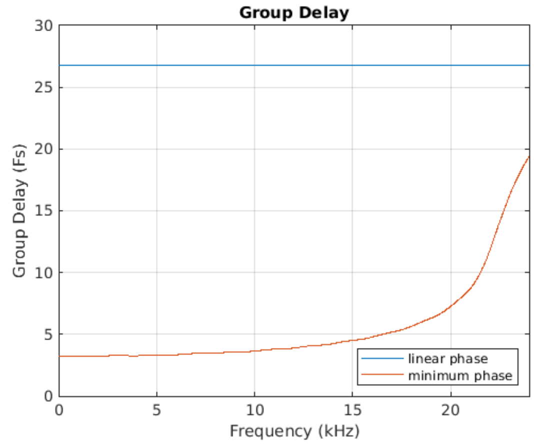


Figure 7-12. Group Delay vs. Frequency

ADC Filter Response—Slow Roll-Off, 48 kHz Sample Rate

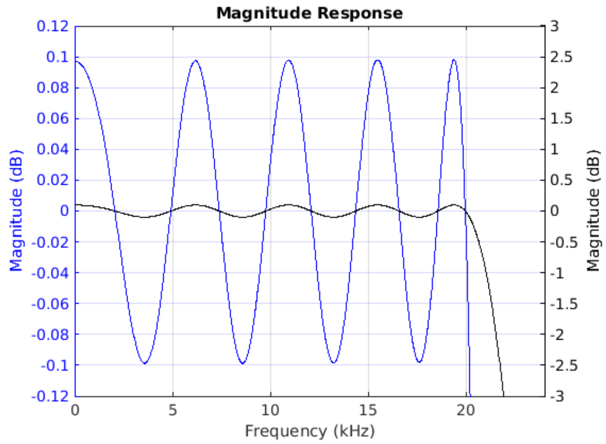


Figure 7-13. Passband Magnitude

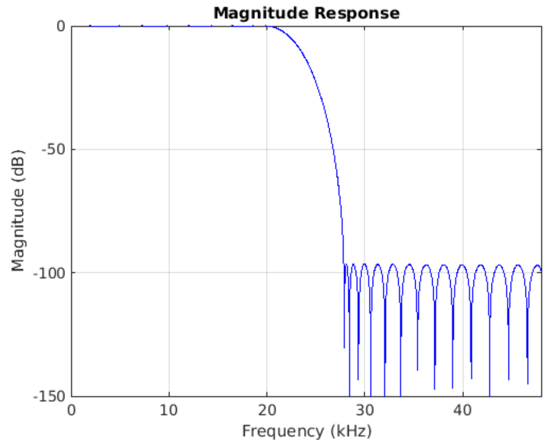


Figure 7-14. Stopband Magnitude

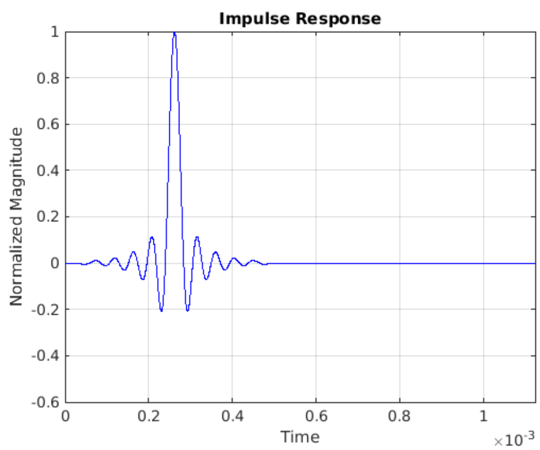


Figure 7-15. Impulse Response—Linear Phase

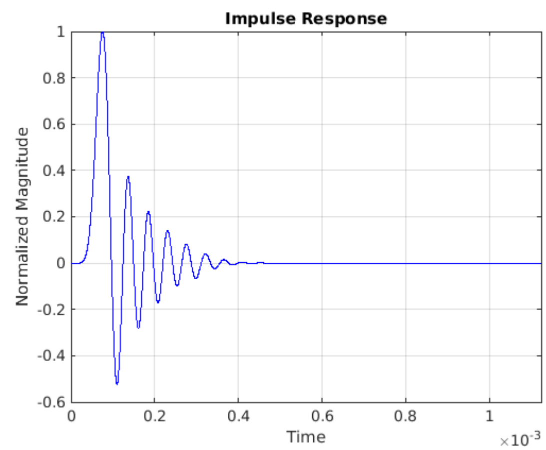


Figure 7-16. Impulse Response—Minimum Phase

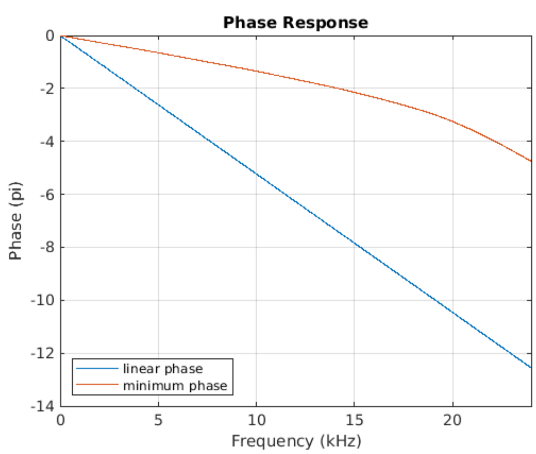


Figure 7-17. Phase vs. Frequency

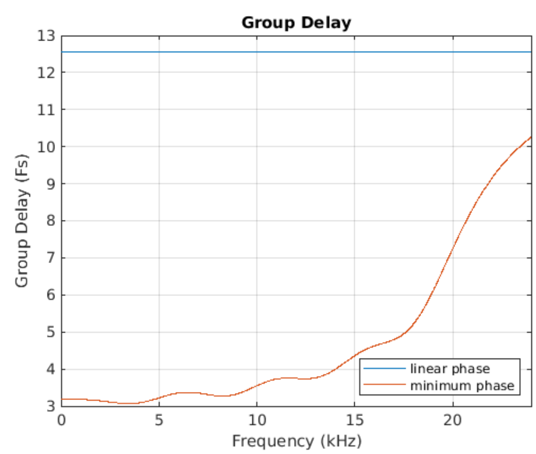


Figure 7-18. Group Delay vs. Frequency

ADC Filter Response—Fast Roll-Off, 96 kHz Sample Rate

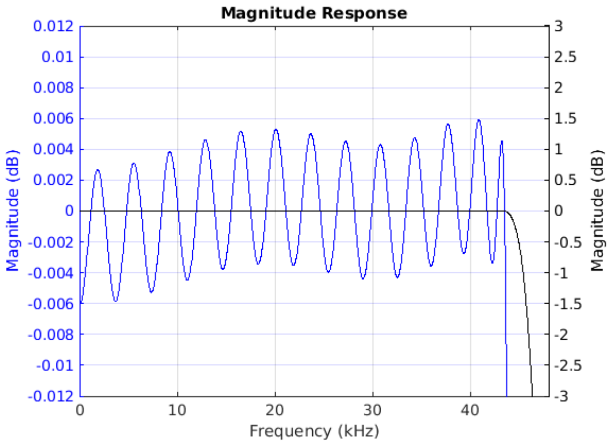


Figure 7-19. Passband Magnitude

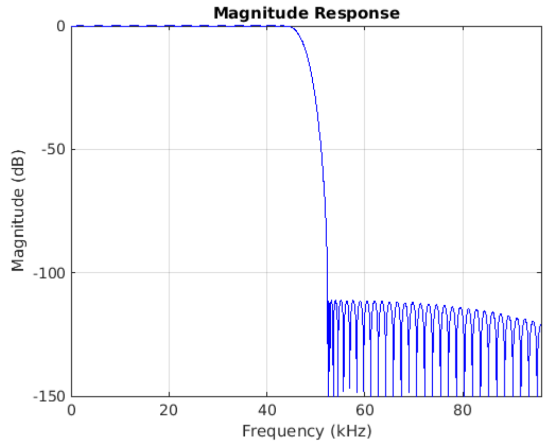


Figure 7-20. Stopband Magnitude

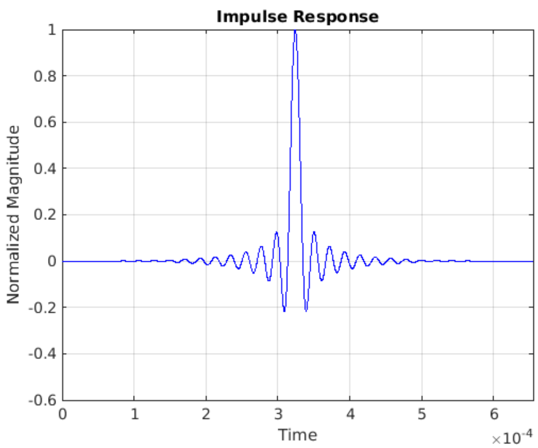


Figure 7-21. Impulse Response—Linear Phase

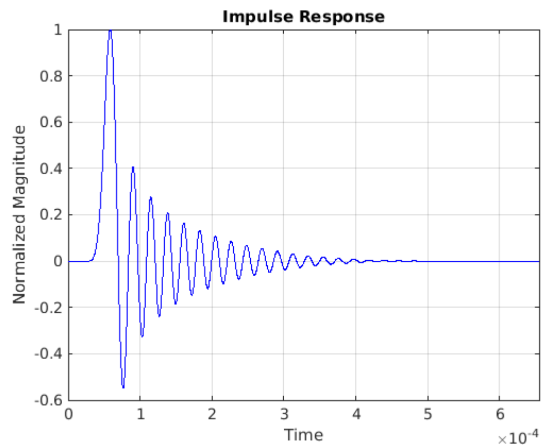


Figure 7-22. Impulse Response—Minimum Phase

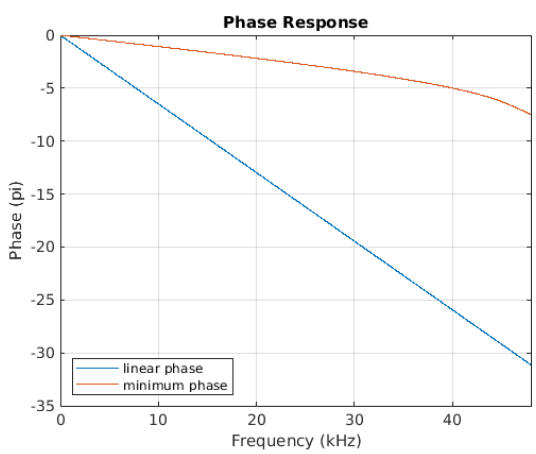


Figure 7-23. Phase vs. Frequency

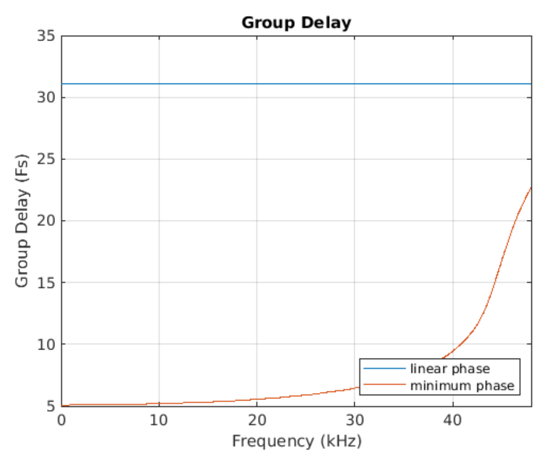


Figure 7-24. Group Delay vs. Frequency

ADC Filter Response—Slow Roll-Off, 96 kHz Sample Rate

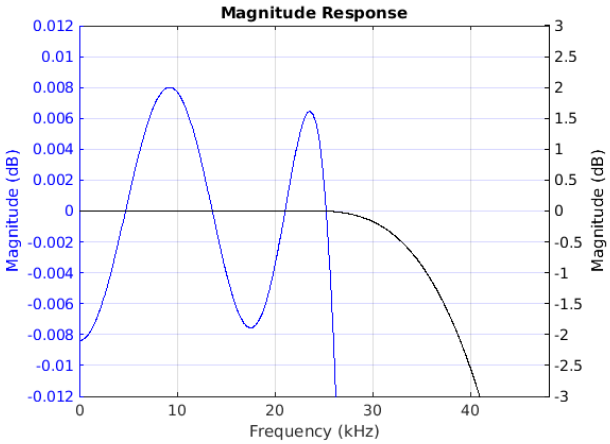


Figure 7-25. Passband Magnitude

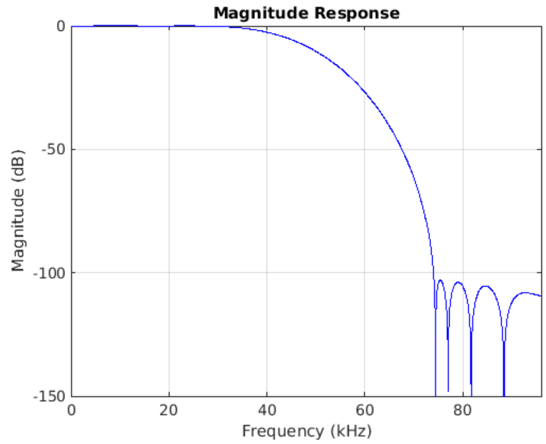


Figure 7-26. Stopband Magnitude

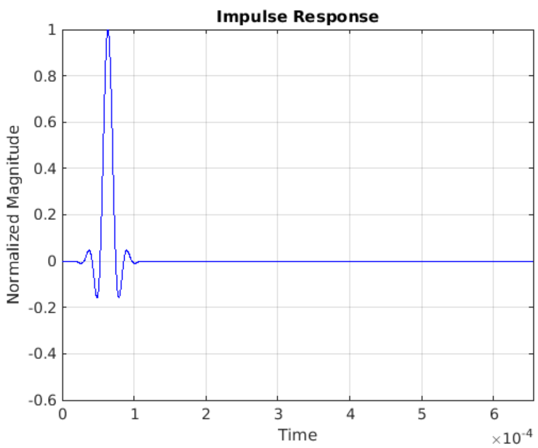


Figure 7-27. Impulse Response—Linear Phase

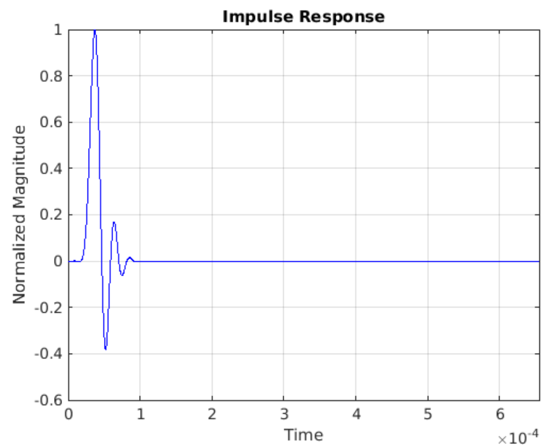


Figure 7-28. Impulse Response—Minimum Phase

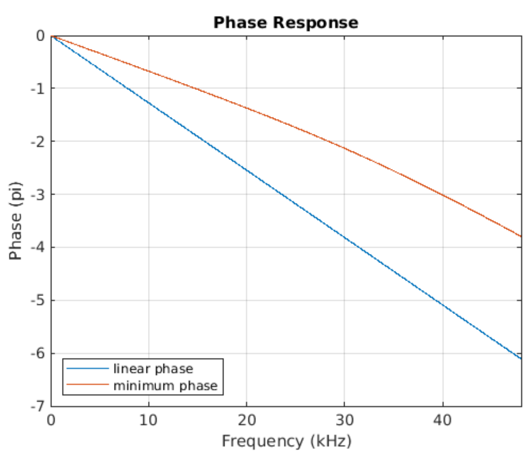


Figure 7-29. Phase vs. Frequency

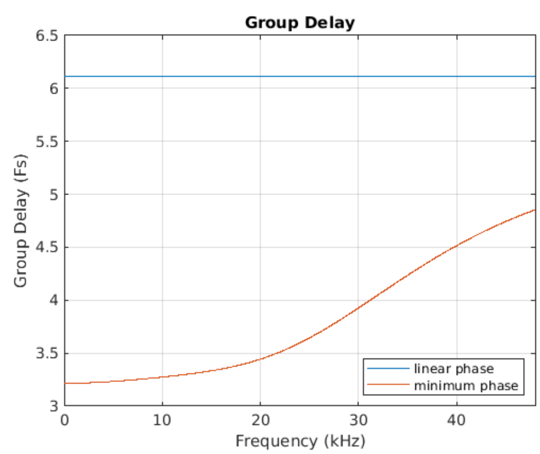


Figure 7-30. Group Delay vs. Frequency

ADC Filter Response—Fast Roll-Off, 192 kHz Sample Rate

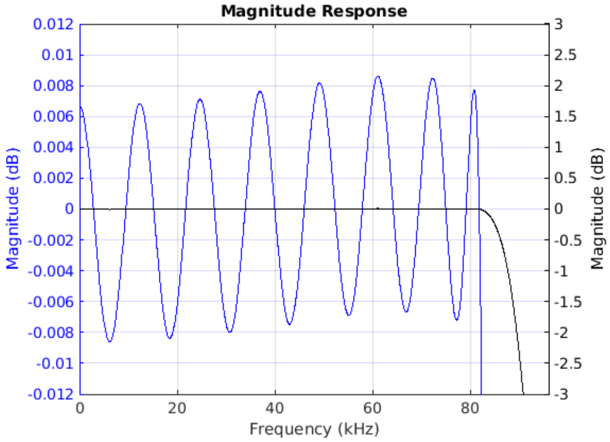


Figure 7-31. Passband Magnitude

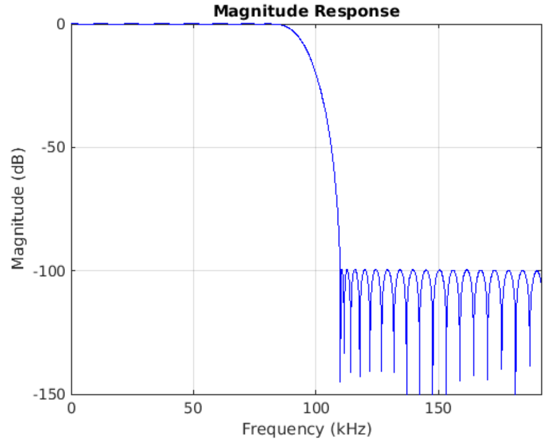


Figure 7-32. Stopband Magnitude

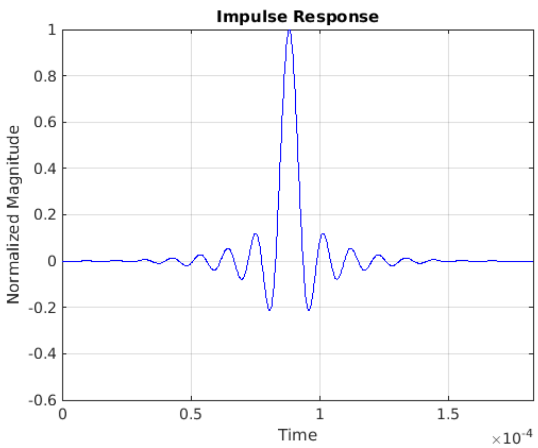


Figure 7-33. Impulse Response—Linear Phase

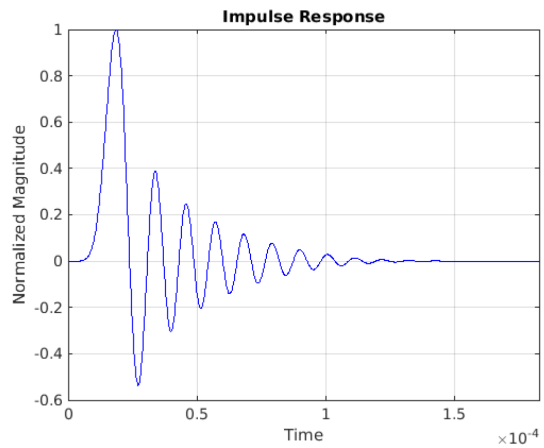


Figure 7-34. Impulse Response—Minimum Phase

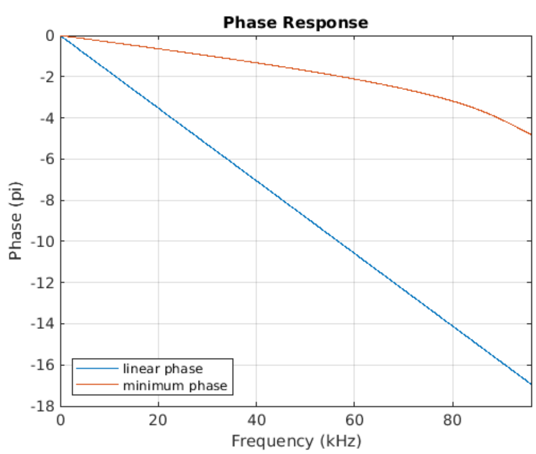


Figure 7-35. Phase vs. Frequency

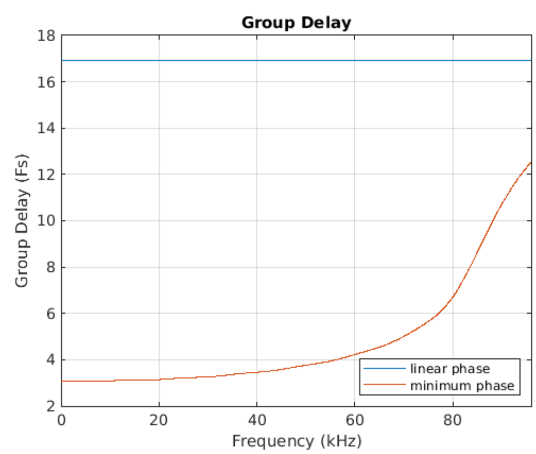


Figure 7-36. Group Delay vs. Frequency

ADC Filter Response—Slow Roll-Off, 192 kHz Sample Rate

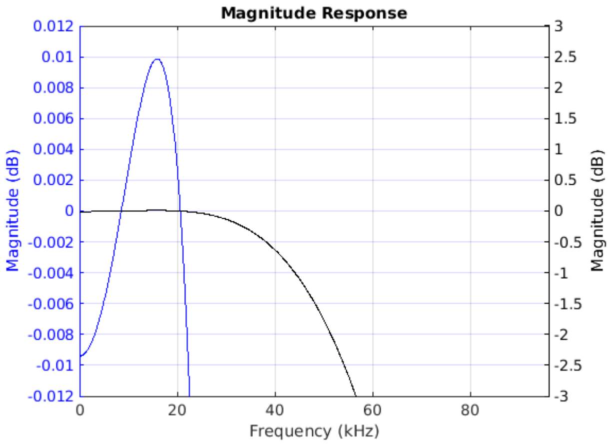


Figure 7-37. Passband Magnitude

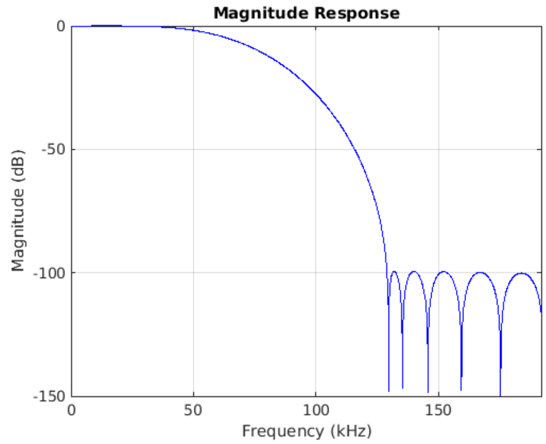


Figure 7-38. Stopband Magnitude

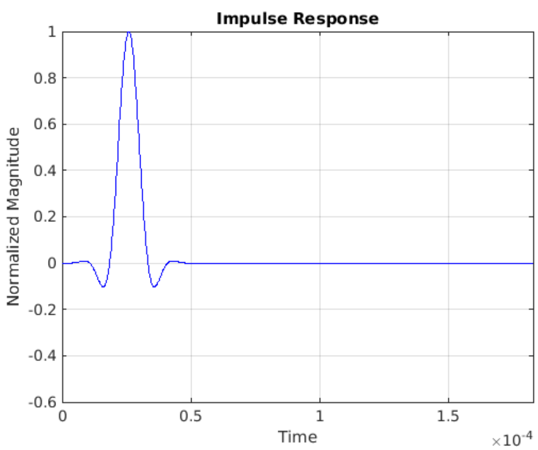


Figure 7-39. Impulse Response—Linear Phase

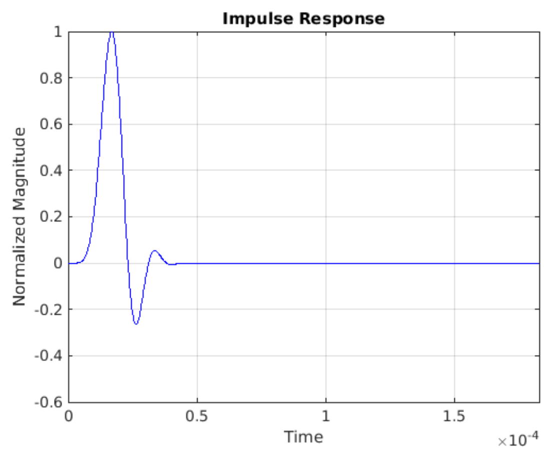


Figure 7-40. Impulse Response—Minimum Phase

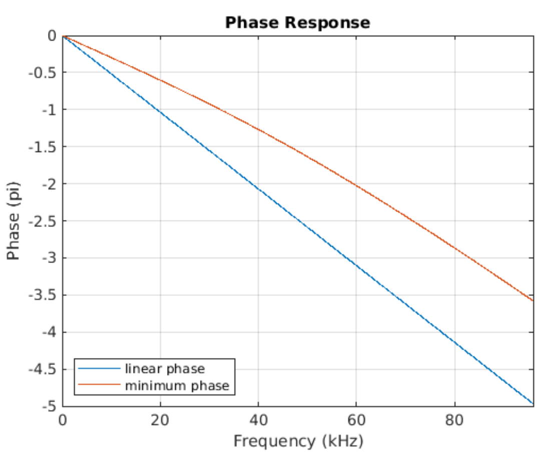


Figure 7-41. Phase vs. Frequency

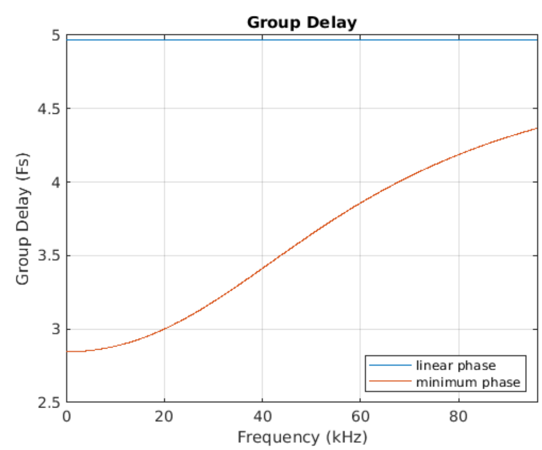


Figure 7-42. Group Delay vs. Frequency

ADC Filter Response—Fast Roll-Off, 384 kHz Sample Rate

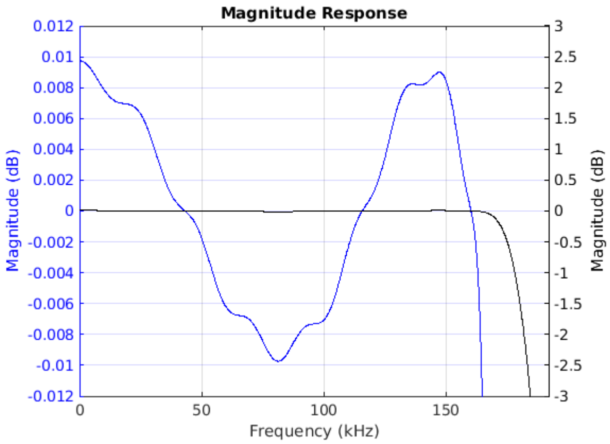


Figure 7-43. Passband Magnitude

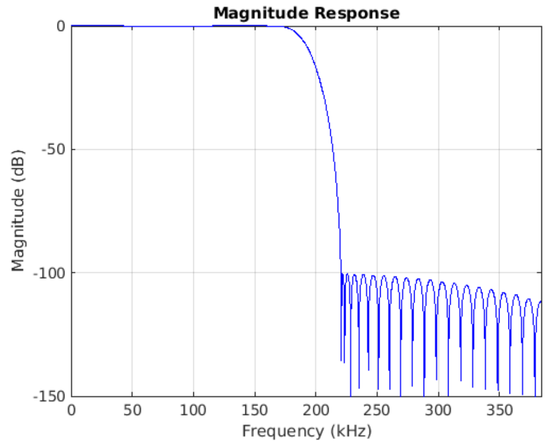


Figure 7-44. Stopband Magnitude

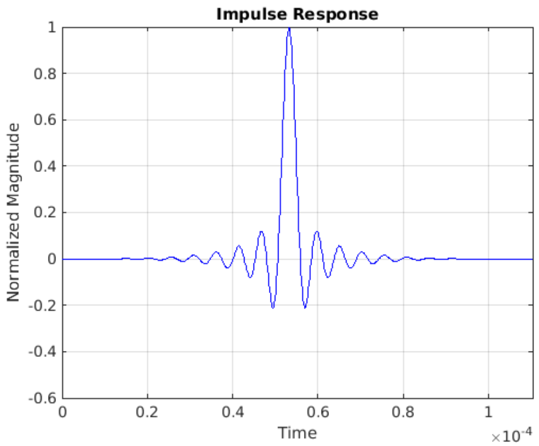


Figure 7-45. Impulse Response—Linear Phase

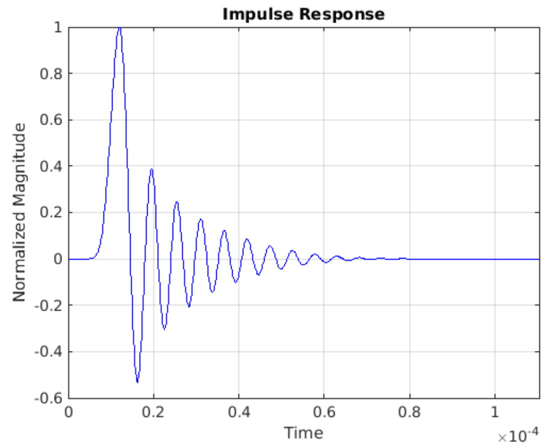


Figure 7-46. Impulse Response—Minimum Phase

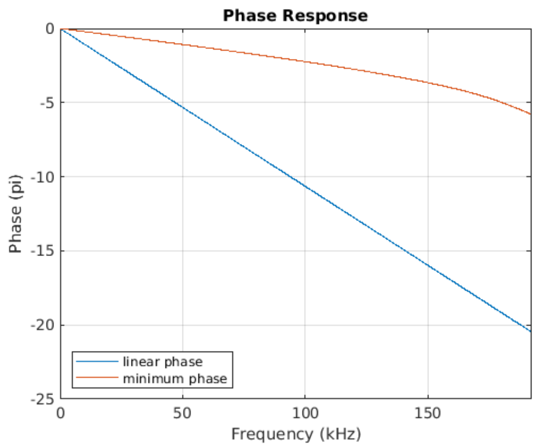


Figure 7-47. Phase vs. Frequency

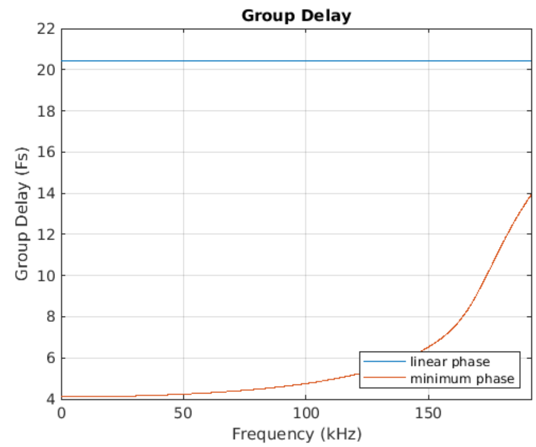


Figure 7-48. Group Delay vs. Frequency

ADC Filter Response—Slow Roll-Off, 384 kHz Sample Rate

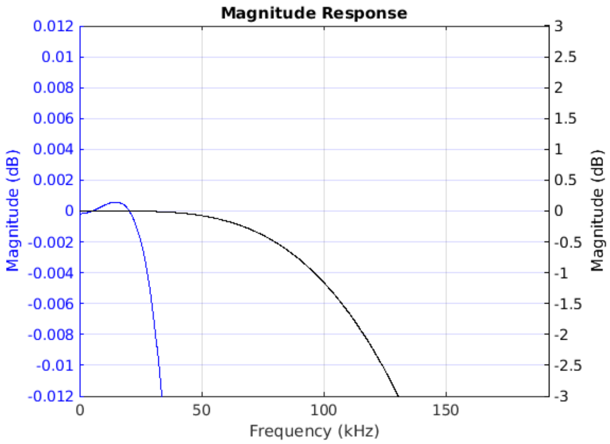


Figure 7-49. Passband Magnitude

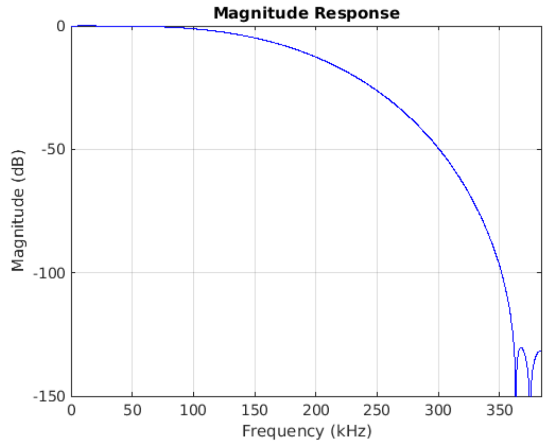


Figure 7-50. Stopband Magnitude

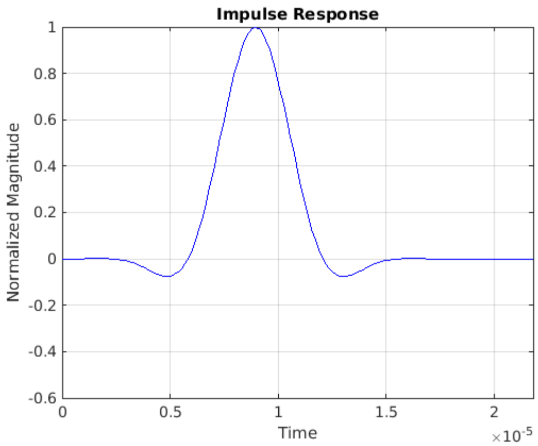


Figure 7-51. Impulse Response—Linear Phase

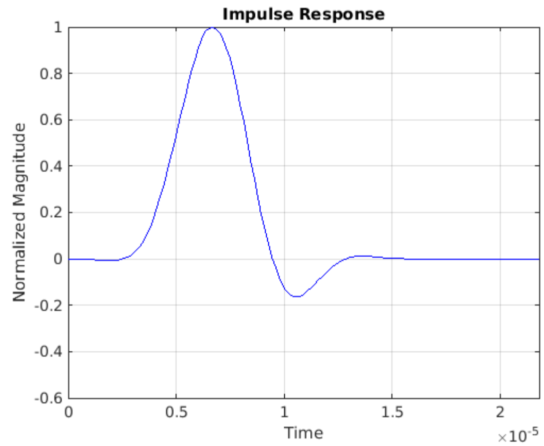


Figure 7-52. Impulse Response—Minimum Phase

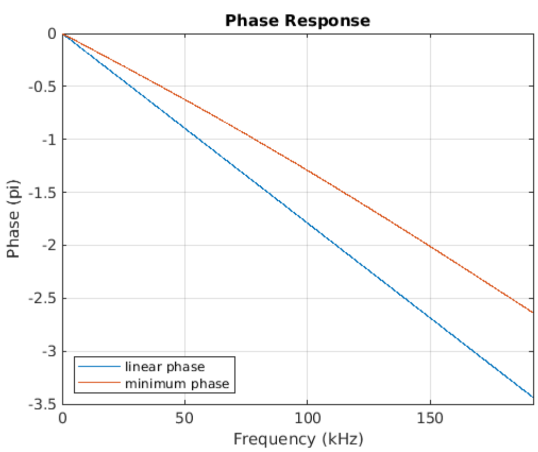


Figure 7-53. Phase vs. Frequency

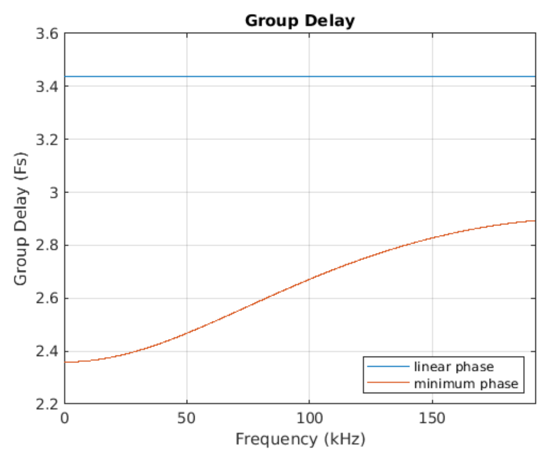


Figure 7-54. Group Delay vs. Frequency

ADC Filter Response—Fast Roll-Off, 768 kHz Sample Rate

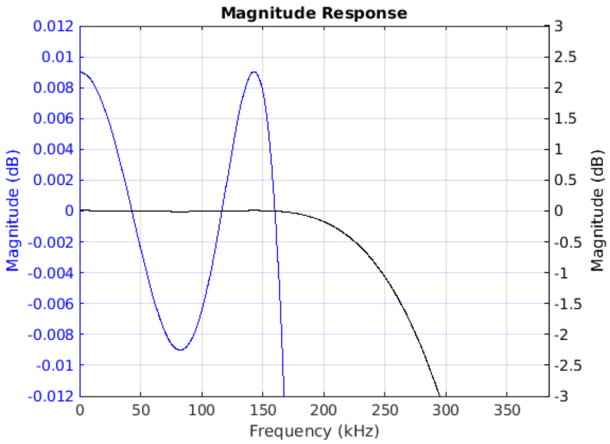


Figure 7-55. Passband Magnitude

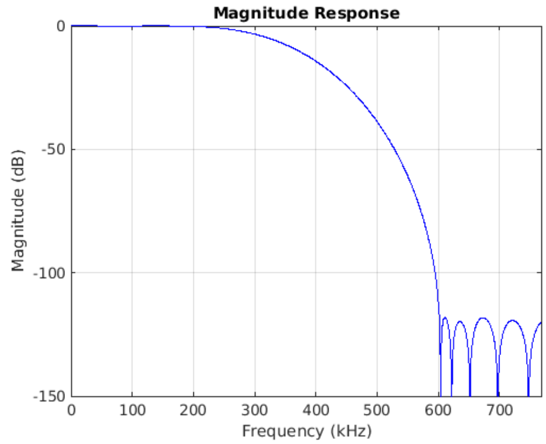


Figure 7-56. Stopband Magnitude

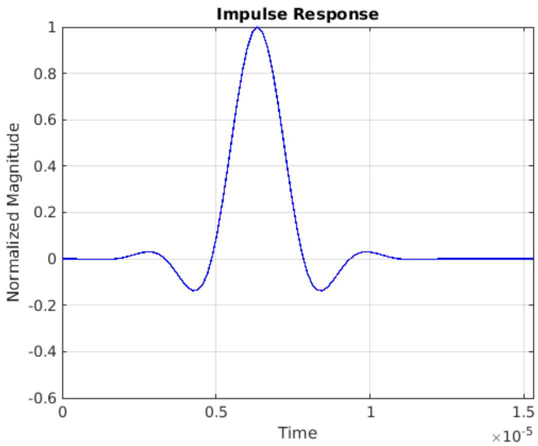


Figure 7-57. Impulse Response—Linear Phase

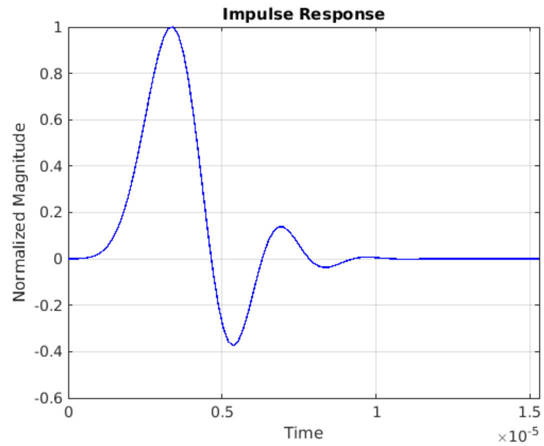


Figure 7-58. Impulse Response—Minimum Phase

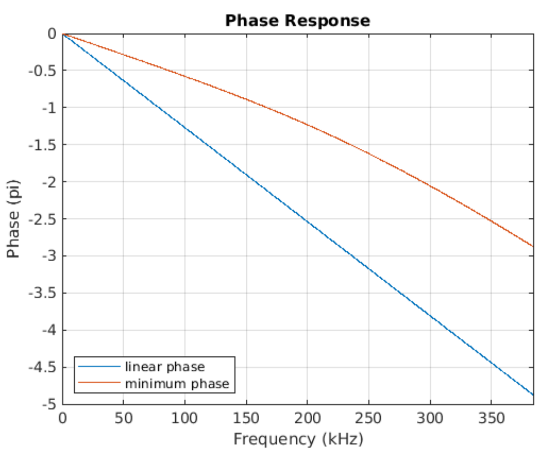


Figure 7-59. Phase vs. Frequency

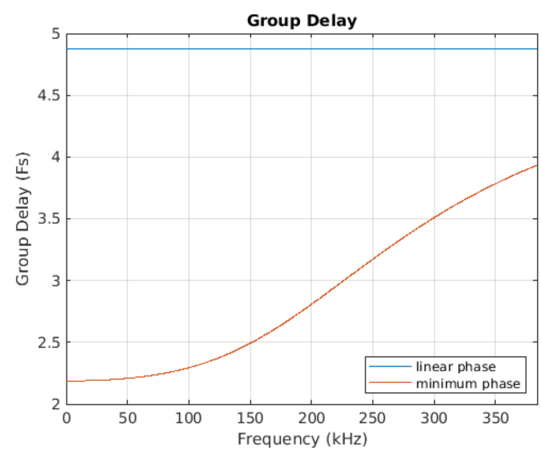


Figure 7-60. Group Delay vs. Frequency

ADC Filter Response—Slow Roll-Off, 768 kHz Sample Rate

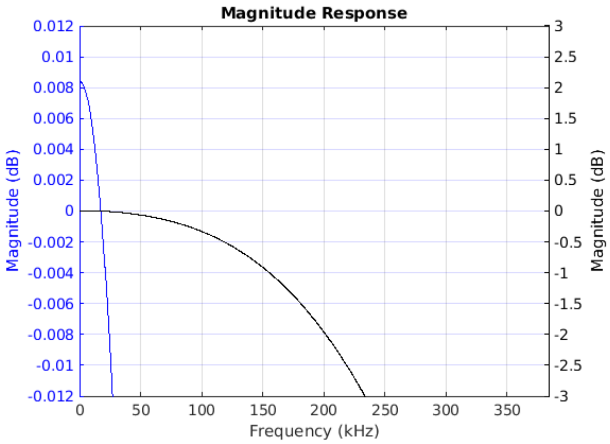


Figure 7-61. Passband Magnitude

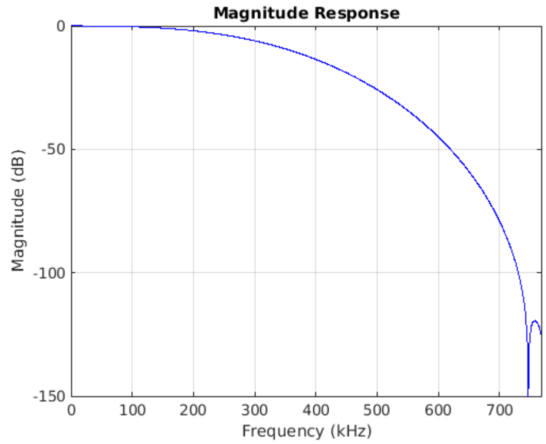


Figure 7-62. Stopband Magnitude

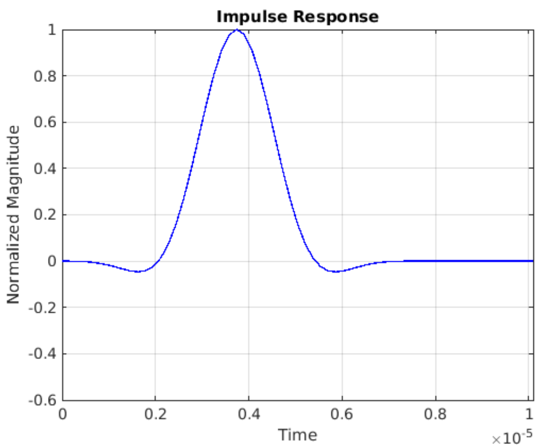


Figure 7-63. Impulse Response—Linear Phase

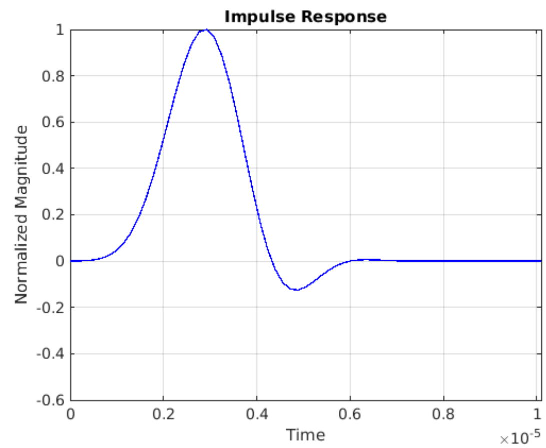


Figure 7-64. Impulse Response—Minimum Phase

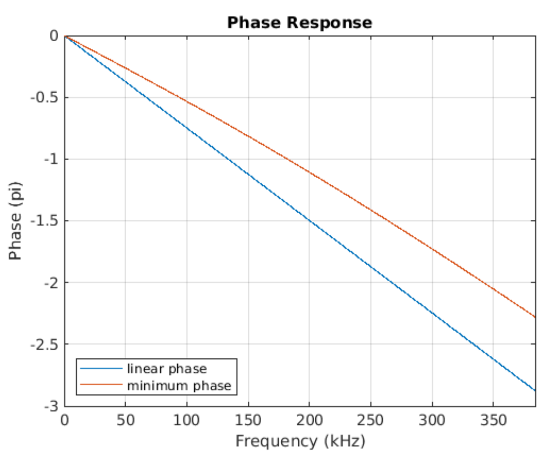


Figure 7-65. Phase vs. Frequency

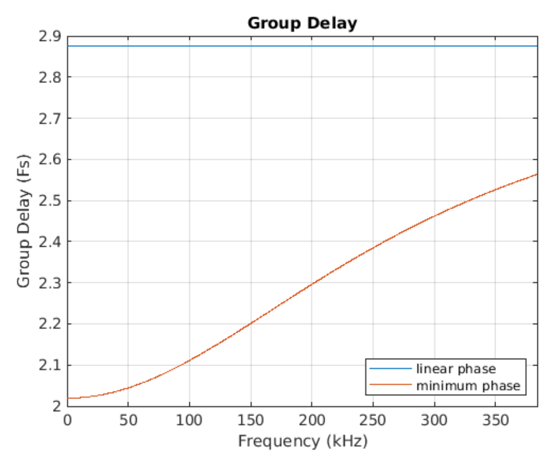


Figure 7-66. Group Delay vs. Frequency

7.2 DAC Filter Response

The DAC filter performance is described in this section. Note that the group-delay plots represent the filter only—see Table 3-8 for full-path latency.

DAC Filter Response—Fast Roll-Off, 32 kHz Sample Rate

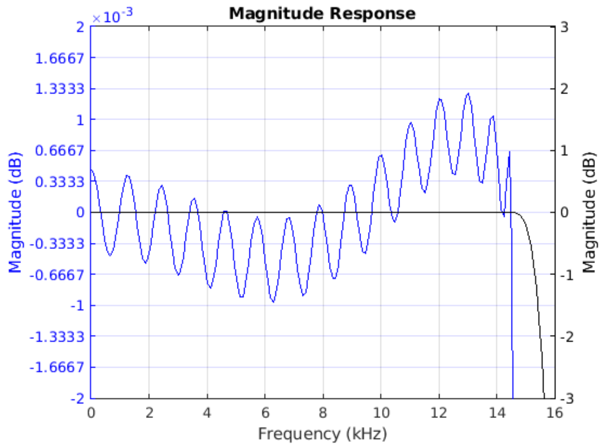


Figure 7-67. Passband Magnitude

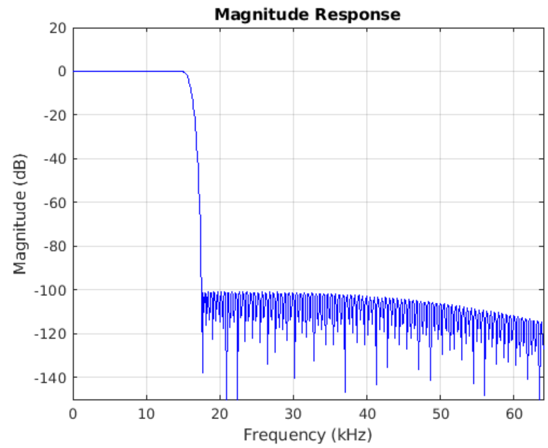


Figure 7-68. Stopband Magnitude

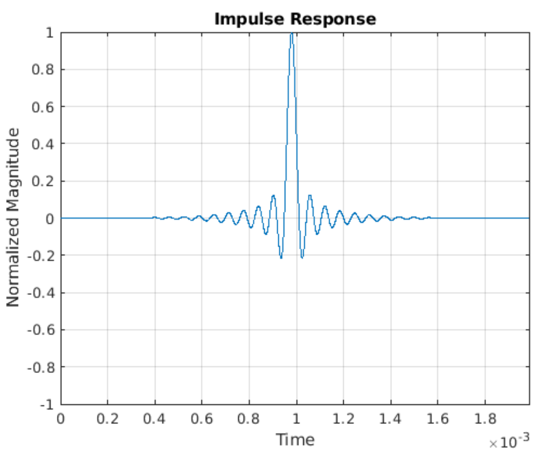


Figure 7-69. Impulse Response—Linear Phase

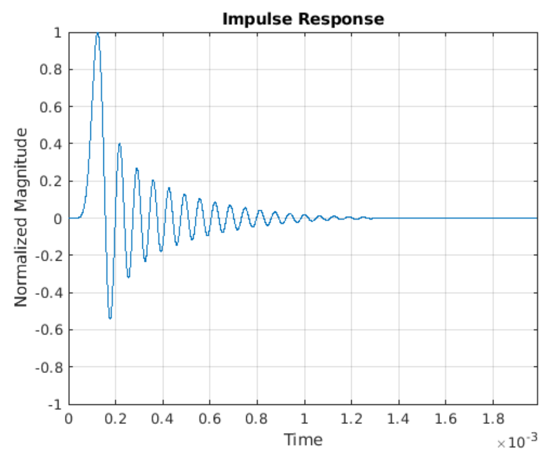


Figure 7-70. Impulse Response—Minimum Phase

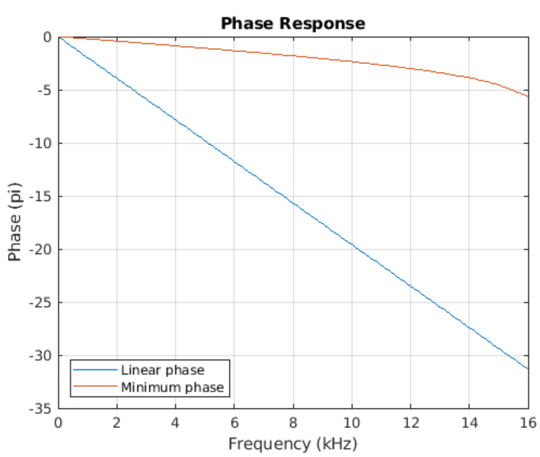


Figure 7-71. Phase vs. Frequency

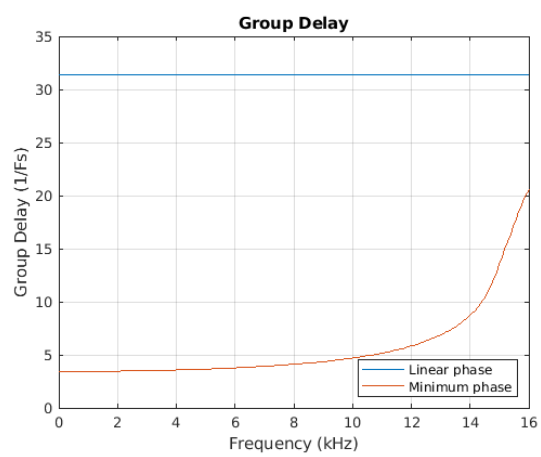


Figure 7-72. Group Delay vs. Frequency

DAC Filter Response—Fast Roll-Off, 48 kHz Sample Rate

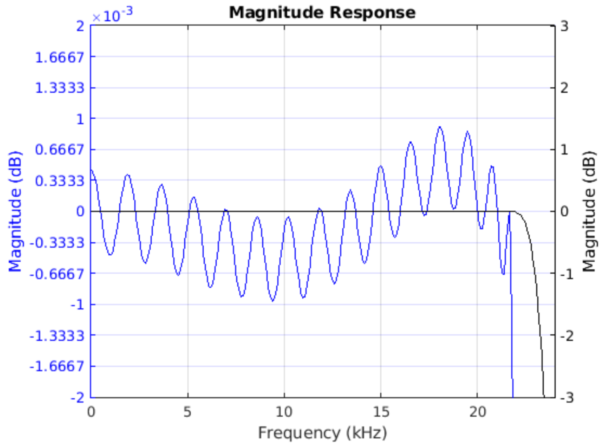


Figure 7-73. Passband Magnitude

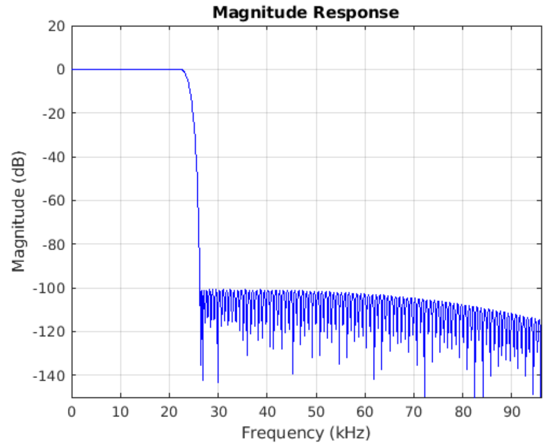


Figure 7-74. Stopband Magnitude

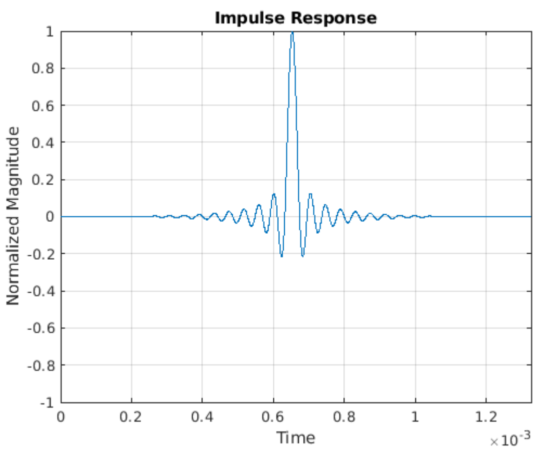


Figure 7-75. Impulse Response—Linear Phase

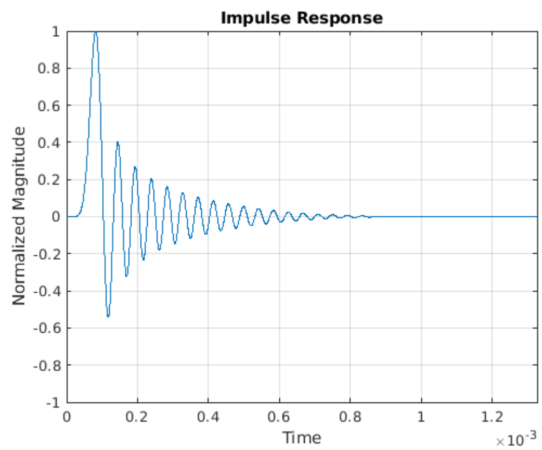


Figure 7-76. Impulse Response—Minimum Phase

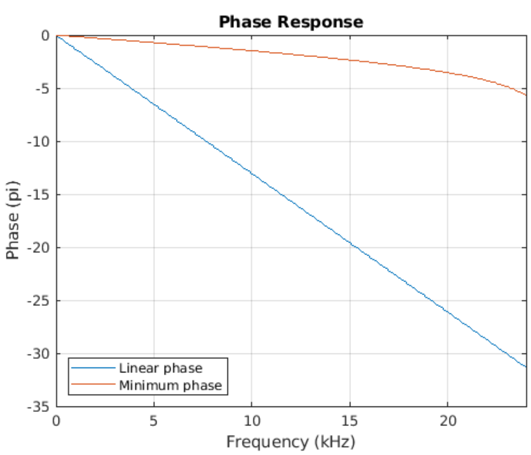


Figure 7-77. Phase vs. Frequency

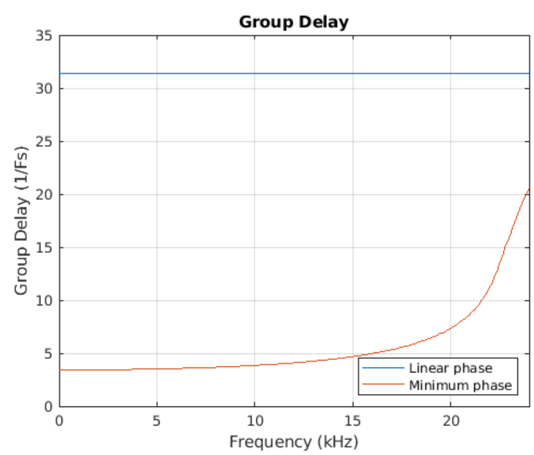


Figure 7-78. Group Delay vs. Frequency

DAC Filter Response—Slow Roll-Off, 48 kHz Sample Rate

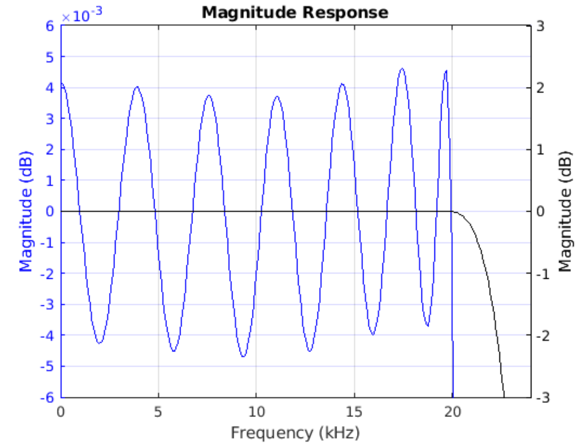


Figure 7-79. Passband Magnitude

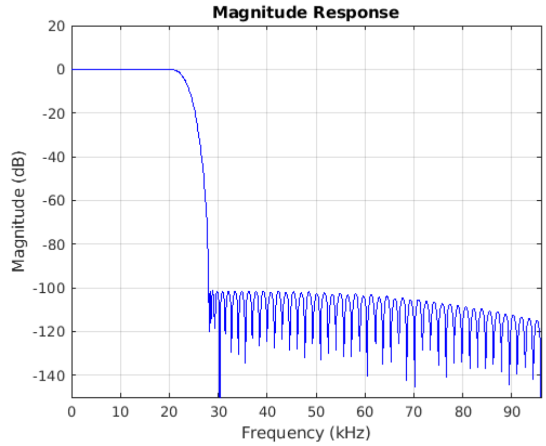


Figure 7-80. Stopband Magnitude

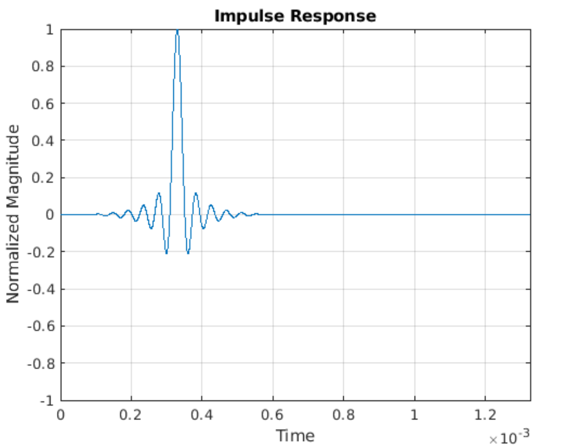


Figure 7-81. Impulse Response—Linear Phase

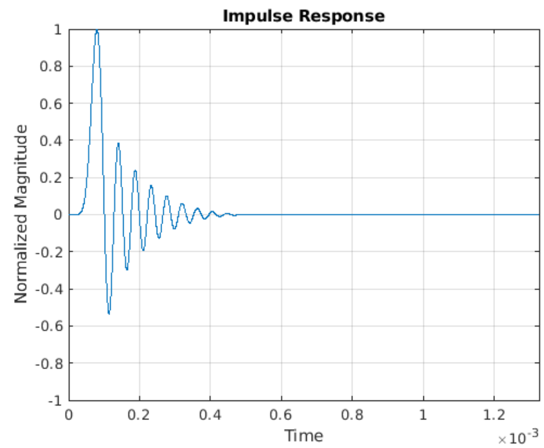


Figure 7-82. Impulse Response—Minimum Phase

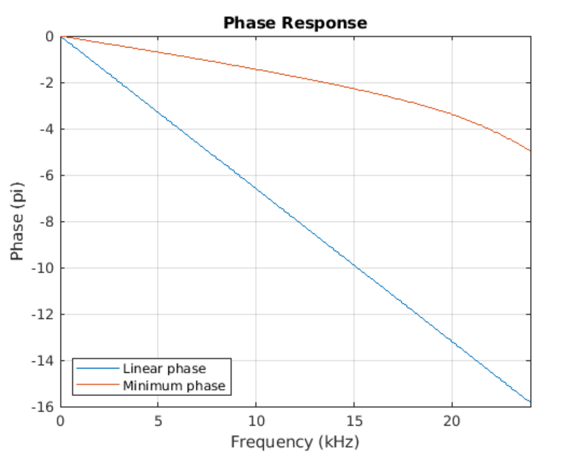


Figure 7-83. Phase vs. Frequency

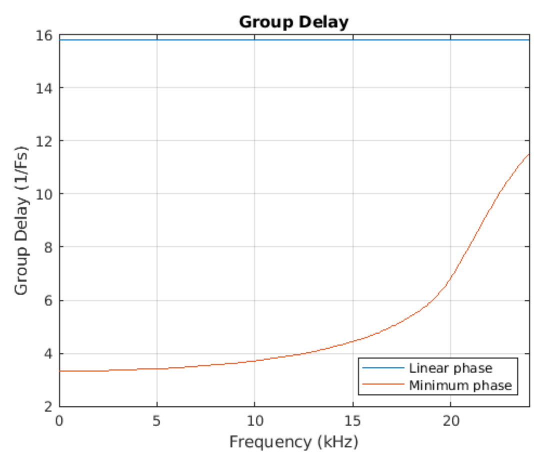


Figure 7-84. Group Delay vs. Frequency

DAC Filter Response—Fast Roll-Off, 96 kHz Sample Rate

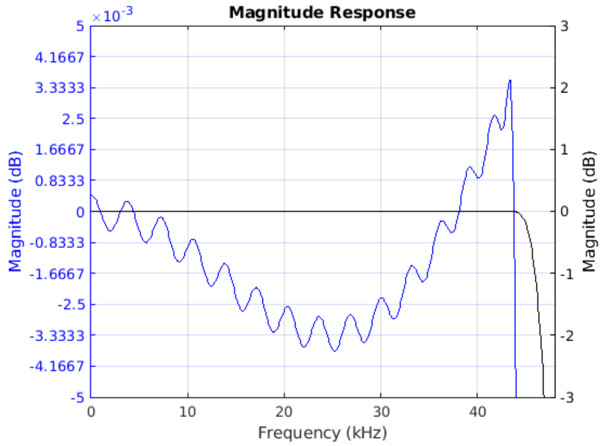


Figure 7-85. Passband Magnitude

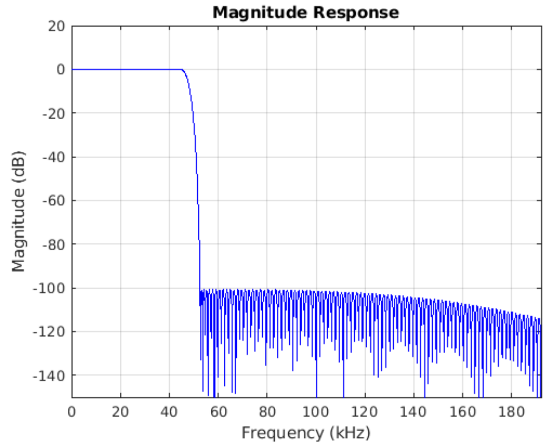


Figure 7-86. Stopband Magnitude

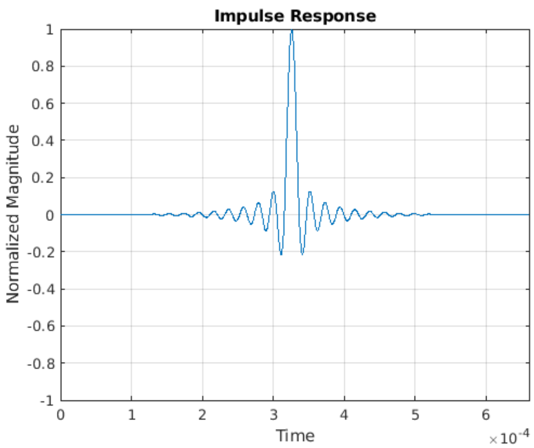


Figure 7-87. Impulse Response—Linear Phase

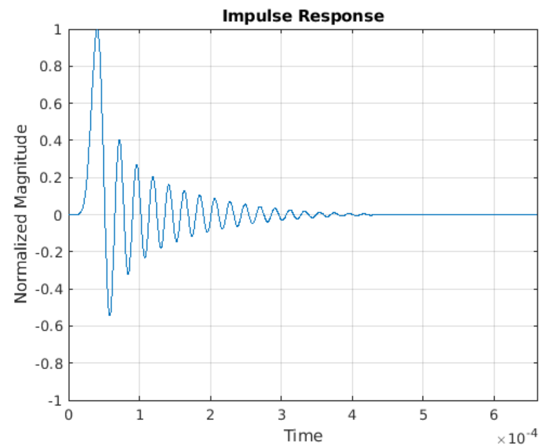


Figure 7-88. Impulse Response—Minimum Phase

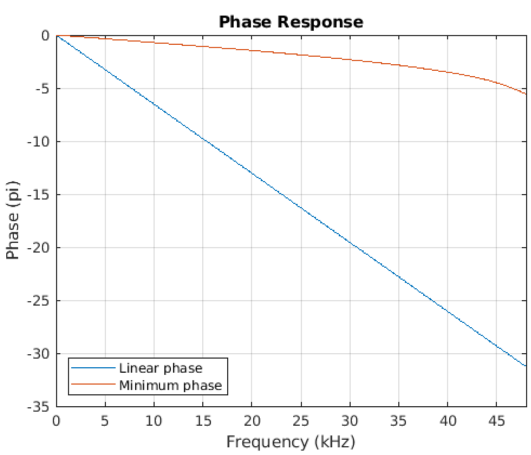


Figure 7-89. Phase vs. Frequency

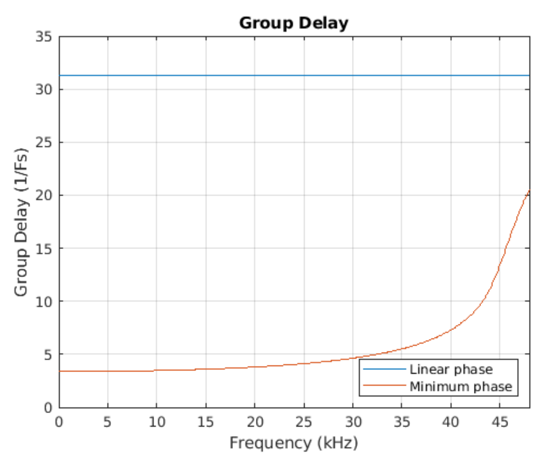


Figure 7-90. Group Delay vs. Frequency

DAC Filter Response—Slow Roll-Off, 96 kHz Sample Rate

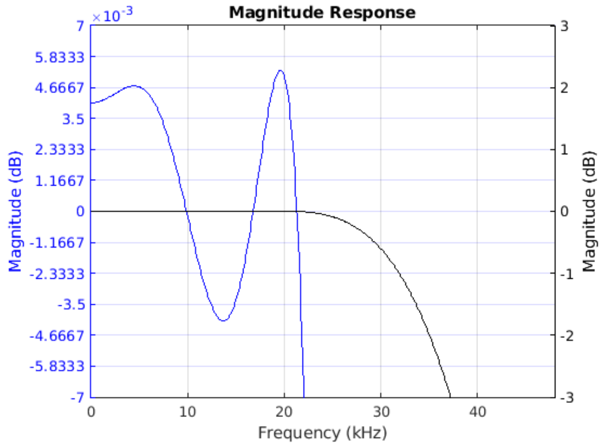


Figure 7-91. Passband Magnitude

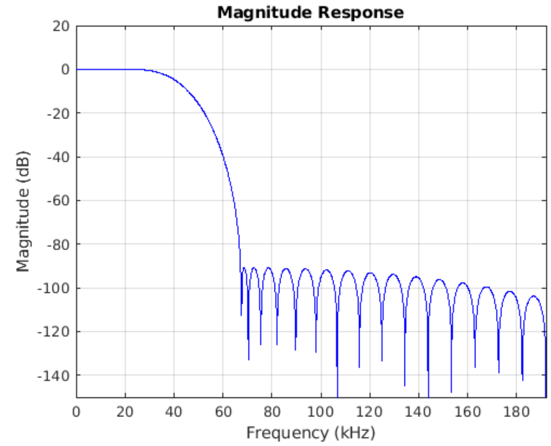


Figure 7-92. Stopband Magnitude

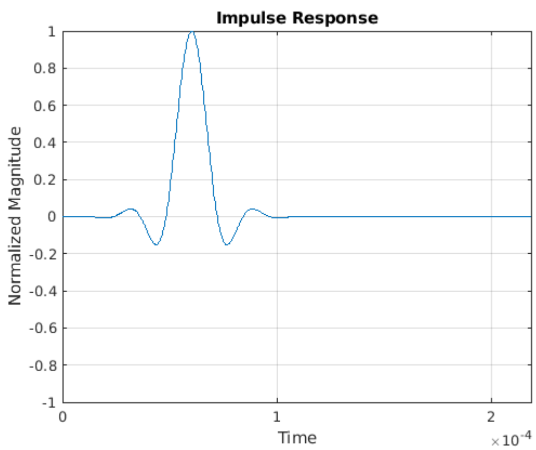


Figure 7-93. Impulse Response—Linear Phase

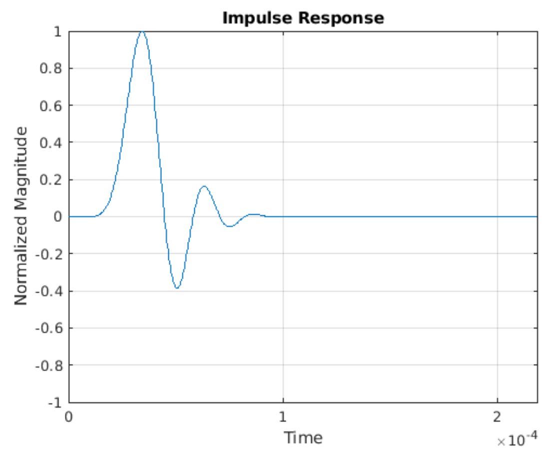


Figure 7-94. Impulse Response—Minimum Phase

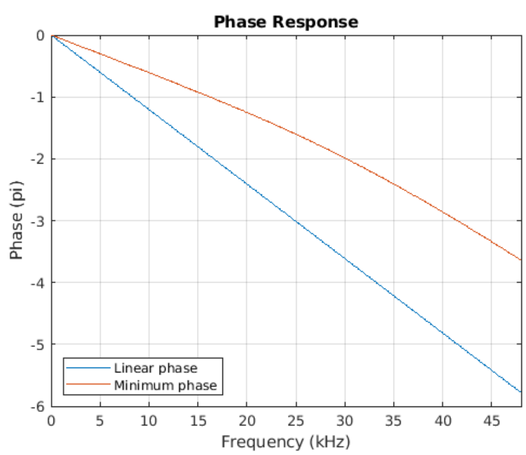


Figure 7-95. Phase vs. Frequency

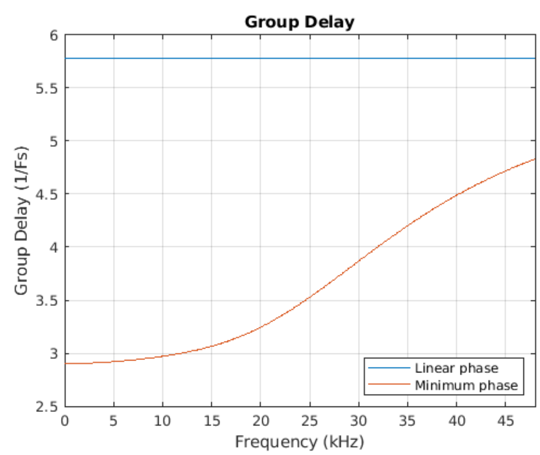


Figure 7-96. Group Delay vs. Frequency

DAC Filter Response—Balanced Roll-Off, 96 kHz Sample Rate

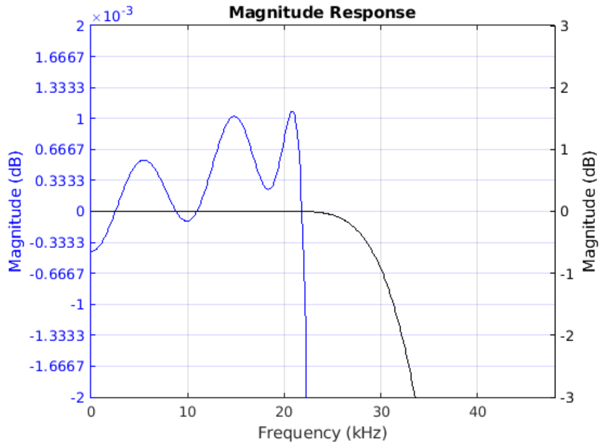


Figure 7-97. Passband Magnitude

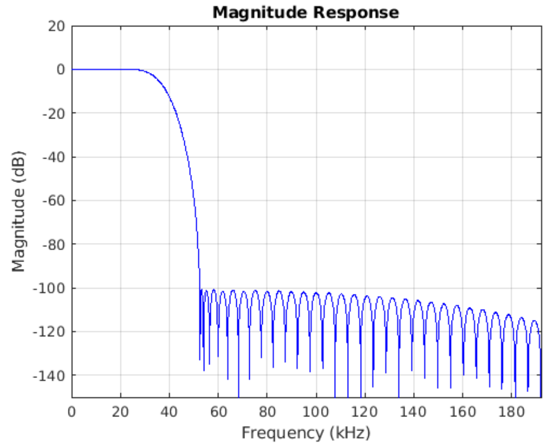


Figure 7-98. Stopband Magnitude

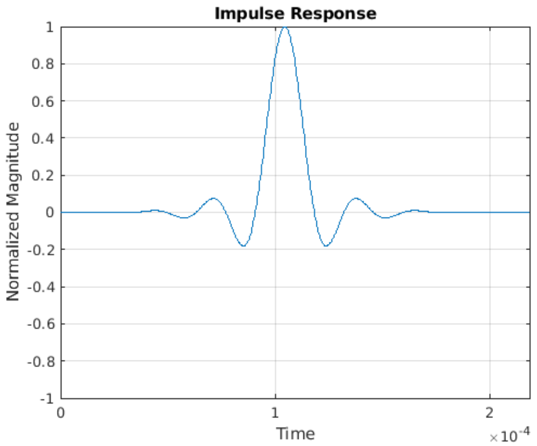


Figure 7-99. Impulse Response—Linear Phase

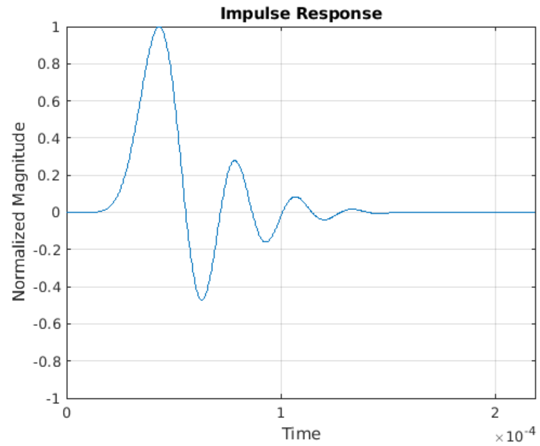


Figure 7-100. Impulse Response—Minimum Phase

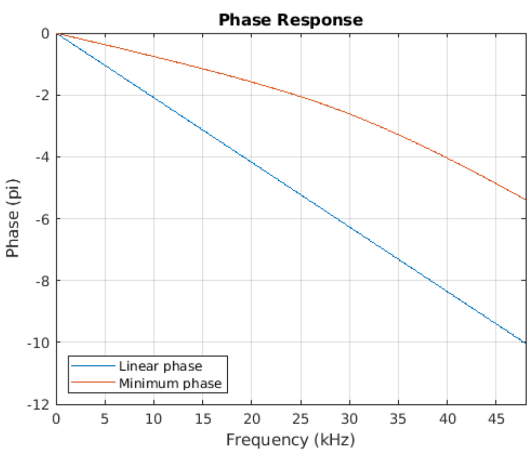


Figure 7-101. Phase vs. Frequency

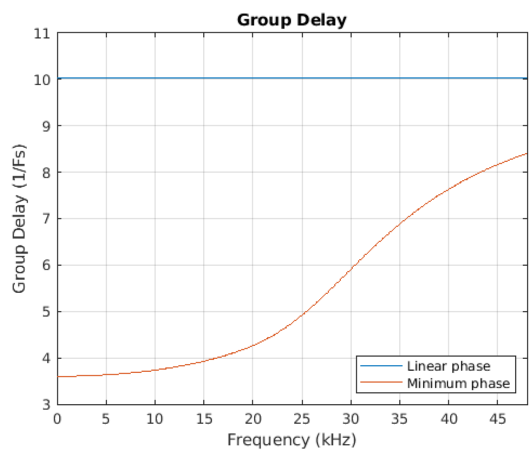


Figure 7-102. Group Delay vs. Frequency

DAC Filter Response—Fast Roll-Off, 192 kHz Sample Rate

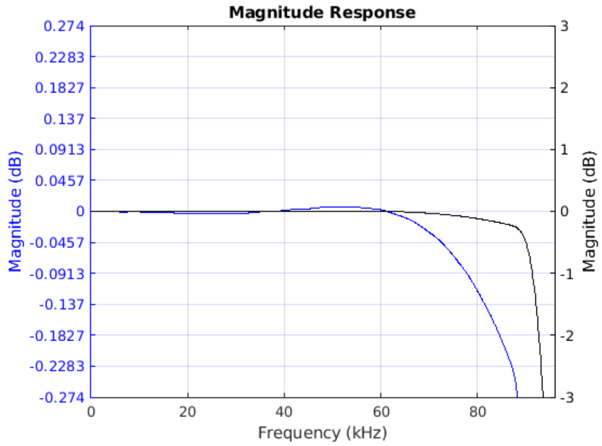


Figure 7-103. Passband Magnitude

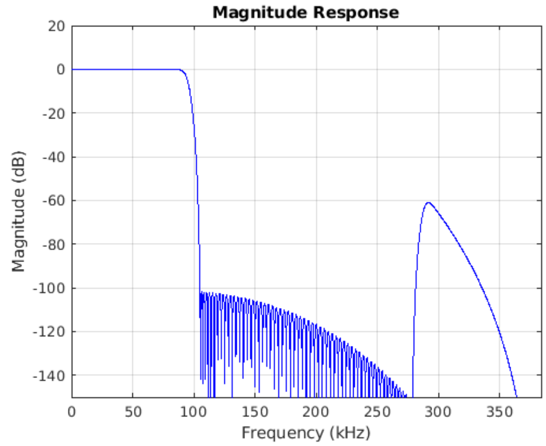


Figure 7-104. Stopband Magnitude

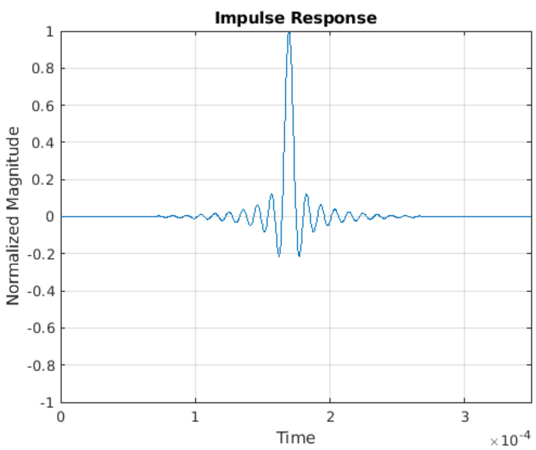


Figure 7-105. Impulse Response—Linear Phase

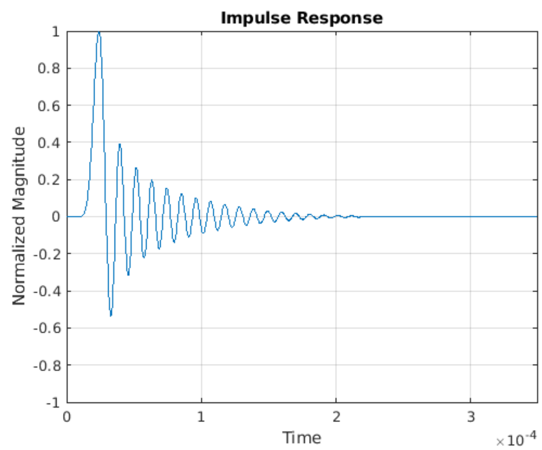


Figure 7-106. Impulse Response—Minimum Phase

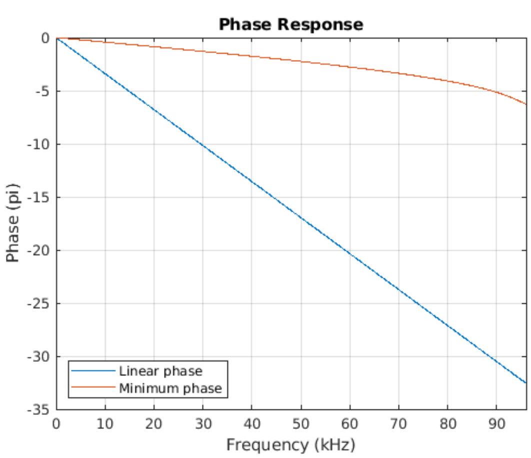


Figure 7-107. Phase vs. Frequency

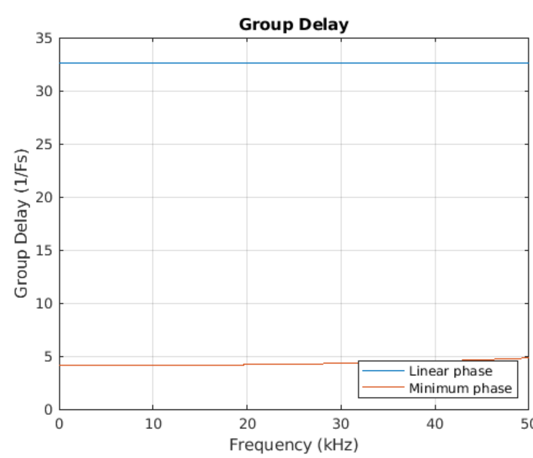


Figure 7-108. Group Delay vs. Frequency

DAC Filter Response—Slow Roll-Off, 192 kHz Sample Rate

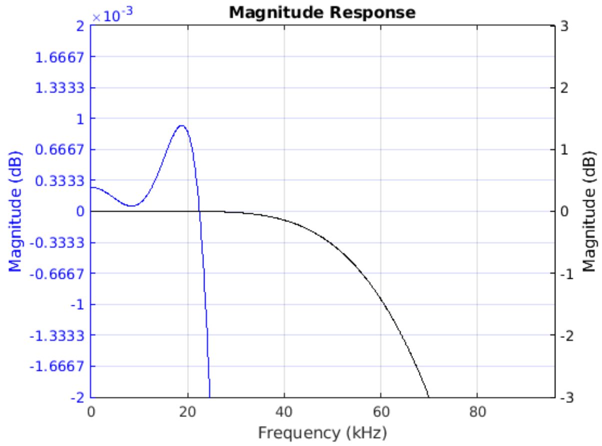


Figure 7-109. Passband Magnitude

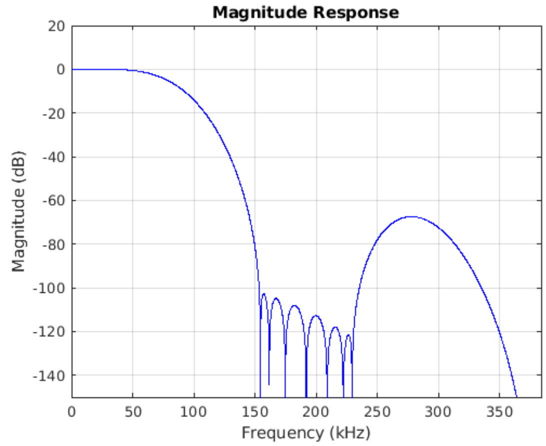


Figure 7-110. Stopband Magnitude

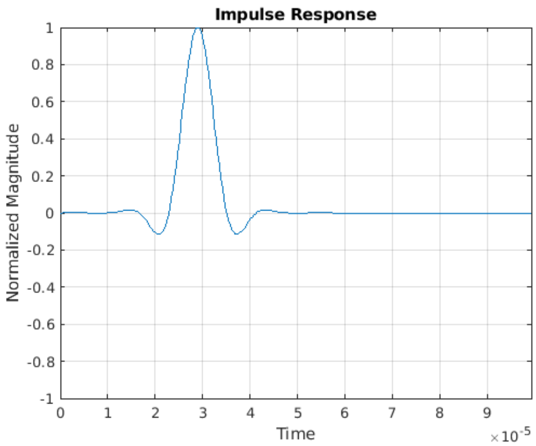


Figure 7-111. Impulse Response—Linear Phase

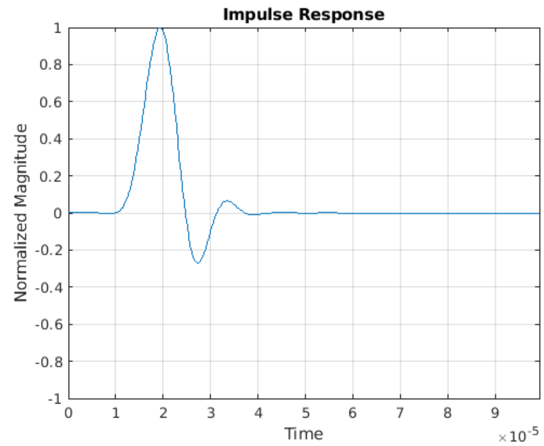


Figure 7-112. Impulse Response—Minimum Phase

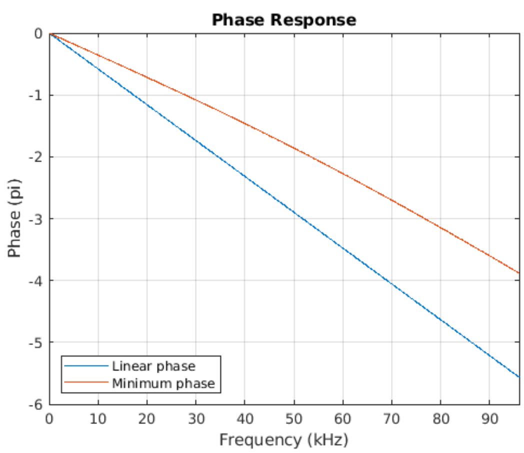


Figure 7-113. Phase vs. Frequency

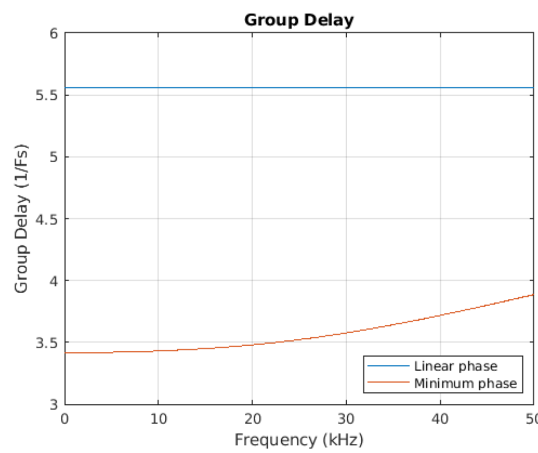


Figure 7-114. Group Delay vs. Frequency

DAC Filter Response—Balanced Roll-Off, 192 kHz Sample Rate

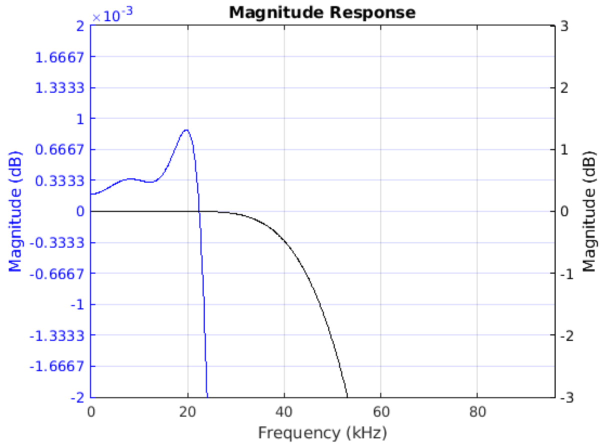


Figure 7-115. Passband Magnitude

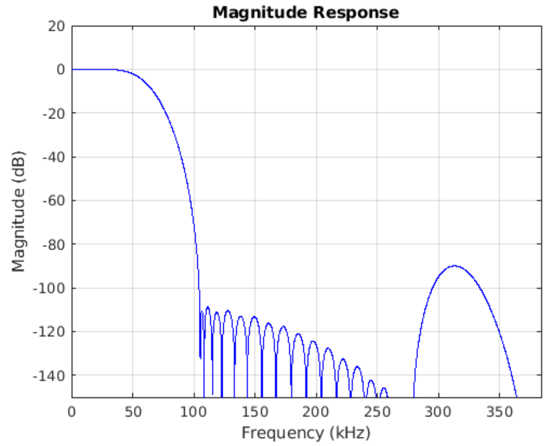


Figure 7-116. Stopband Magnitude

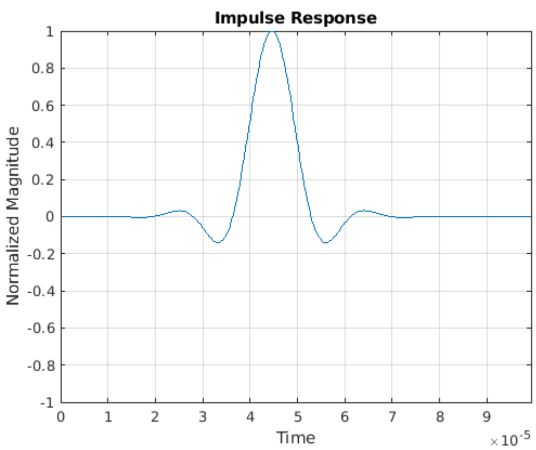


Figure 7-117. Impulse Response—Linear Phase

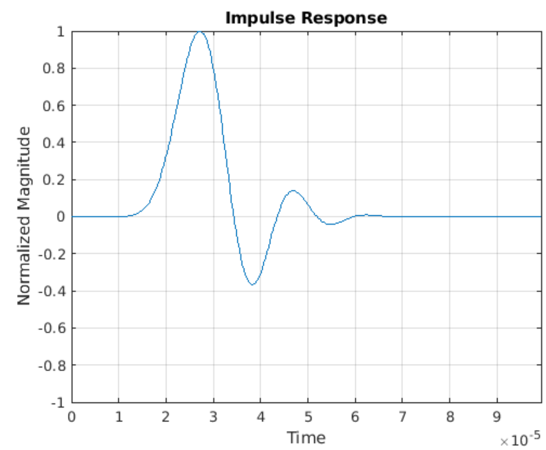


Figure 7-118. Impulse Response—Minimum Phase

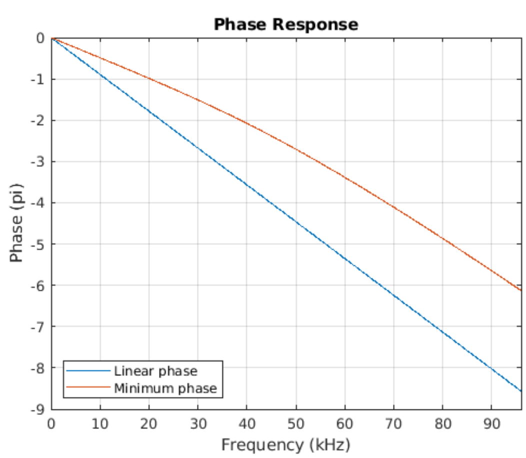


Figure 7-119. Phase vs. Frequency

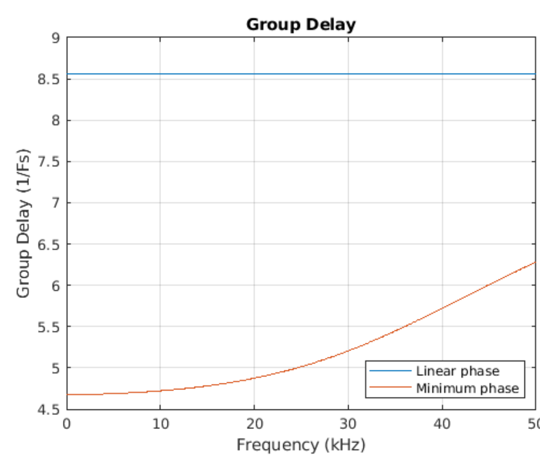


Figure 7-120. Group Delay vs. Frequency

DAC Filter Response—Fast Roll-Off, 384 kHz Sample Rate

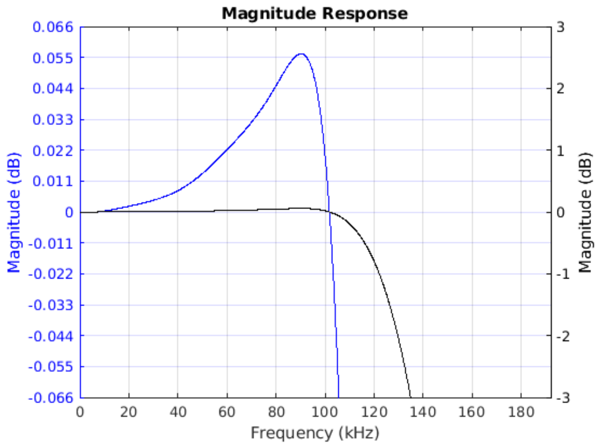


Figure 7-121. Passband Magnitude

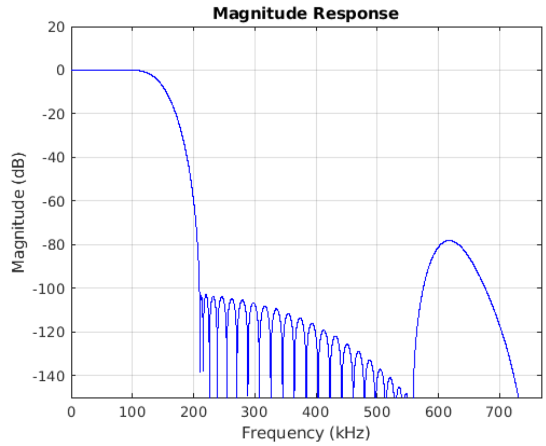


Figure 7-122. Stopband Magnitude

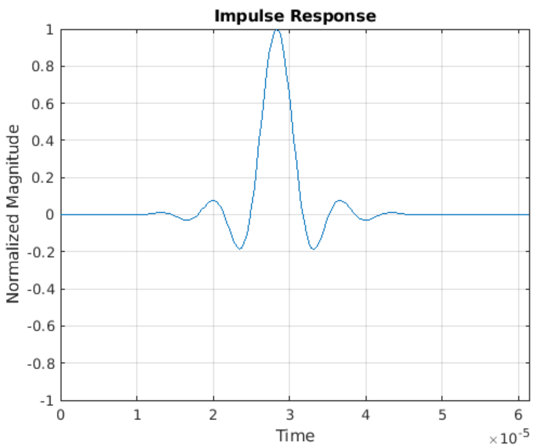


Figure 7-123. Impulse Response—Linear Phase

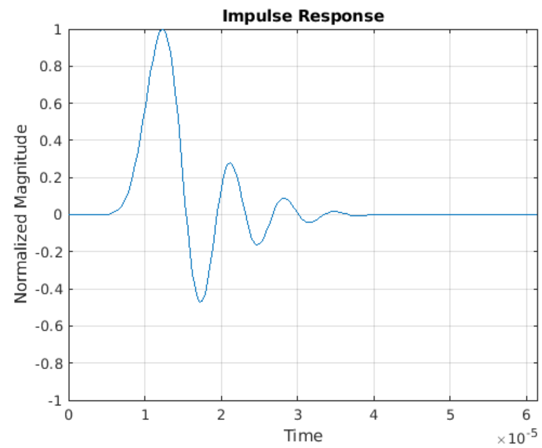


Figure 7-124. Impulse Response—Minimum Phase

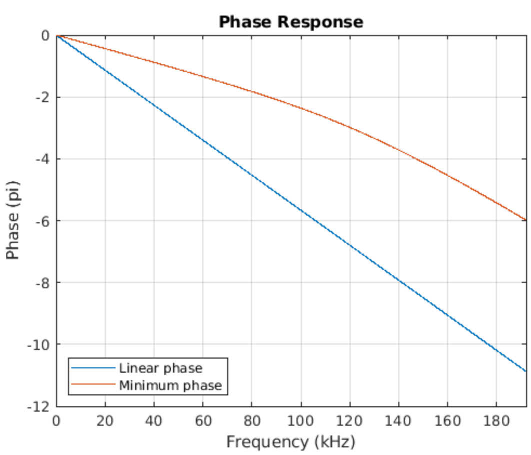


Figure 7-125. Phase vs. Frequency

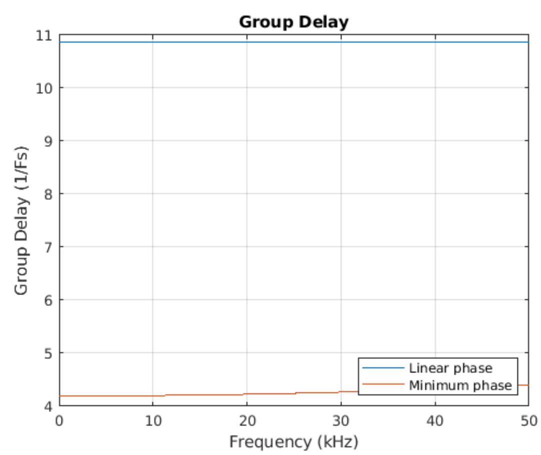


Figure 7-126. Group Delay vs. Frequency

DAC Filter Response—Balanced Roll-Off, 384 kHz Sample Rate

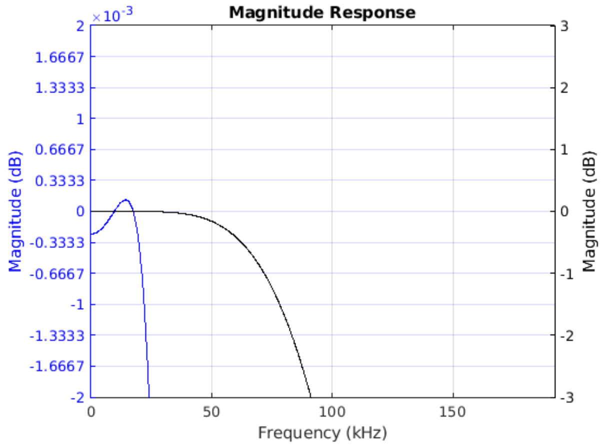


Figure 7-127. Passband Magnitude

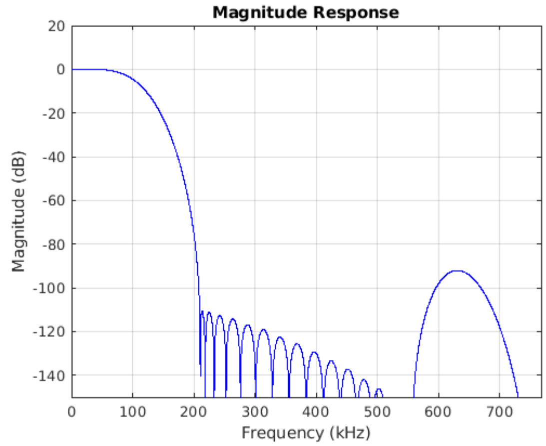


Figure 7-128. Stopband Magnitude

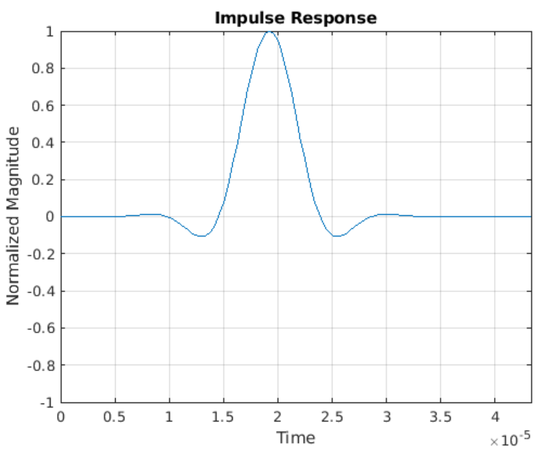


Figure 7-129. Impulse Response—Linear Phase

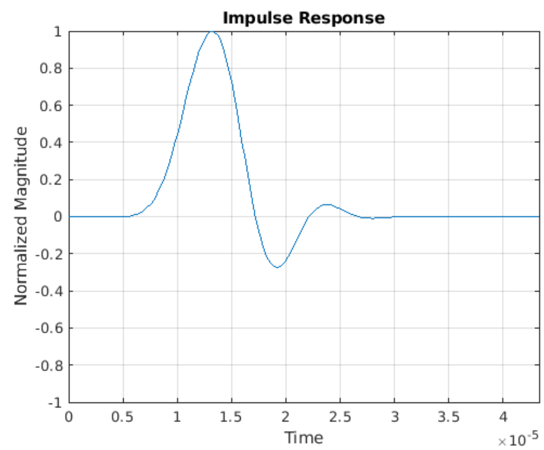


Figure 7-130. Impulse Response—Minimum Phase

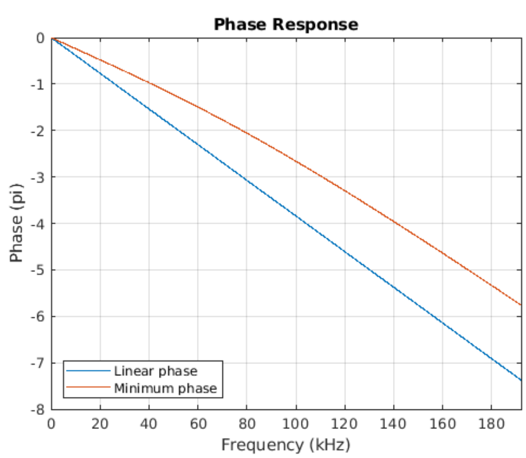


Figure 7-131. Phase vs. Frequency

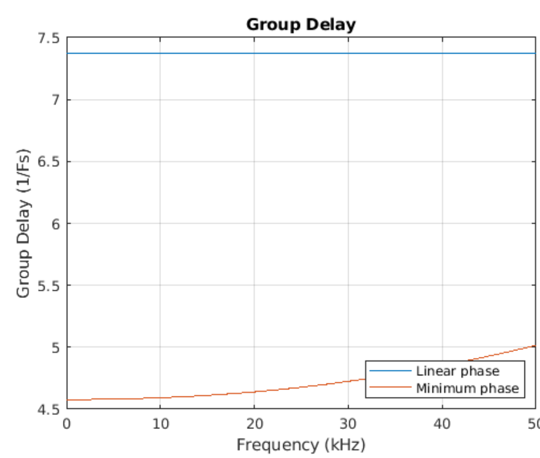


Figure 7-132. Group Delay vs. Frequency

DAC Filter Response—Fast Roll-Off, 768 kHz Sample Rate

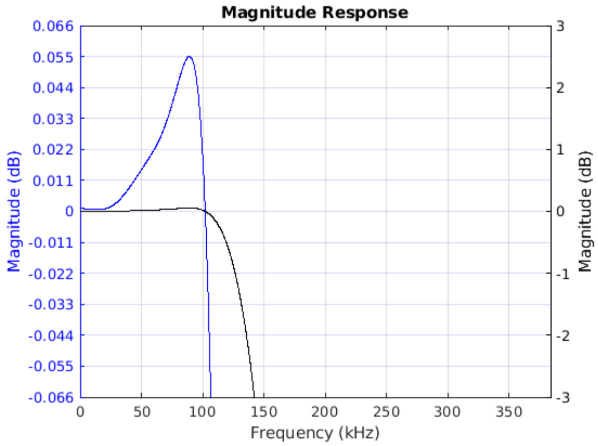


Figure 7-133. Passband Magnitude

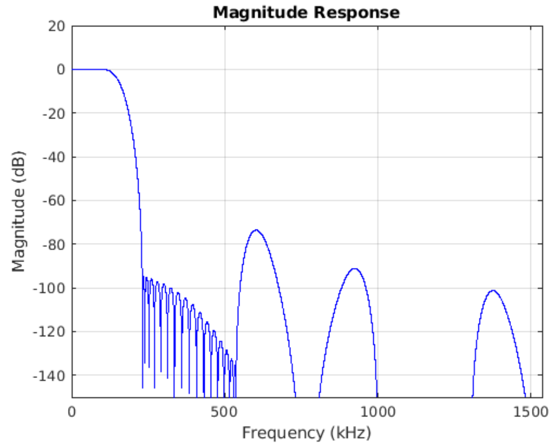


Figure 7-134. Stopband Magnitude

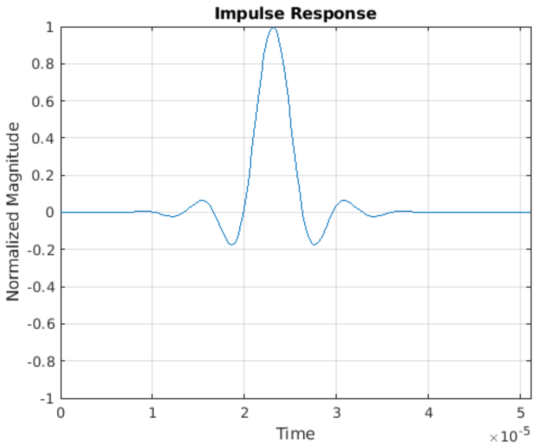


Figure 7-135. Impulse Response—Linear Phase

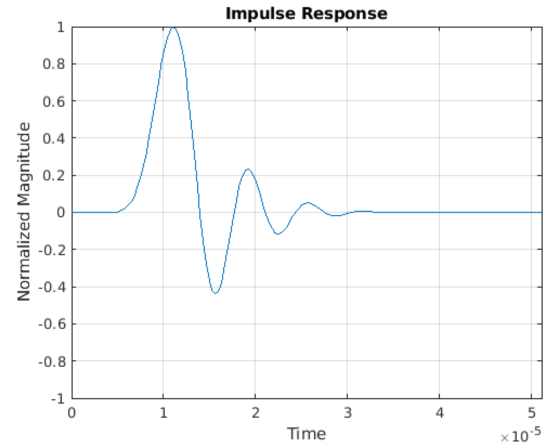


Figure 7-136. Impulse Response—Minimum Phase

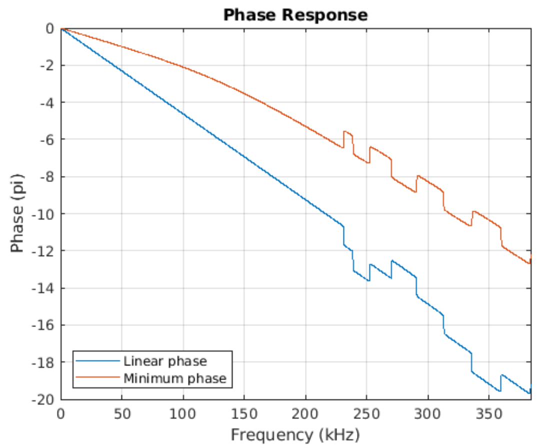


Figure 7-137. Phase vs. Frequency

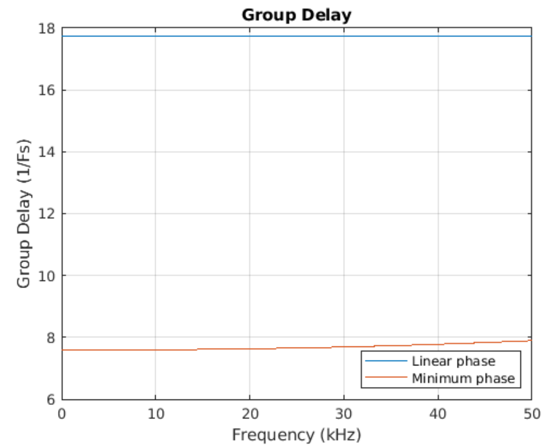


Figure 7-138. Group Delay vs. Frequency

DAC Filter Response—Balanced Roll-Off, 768 kHz Sample Rate

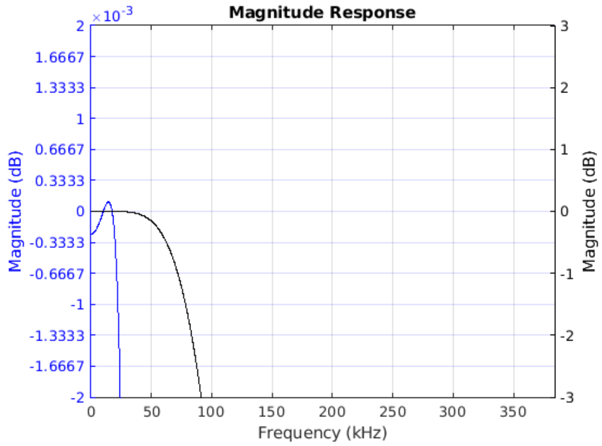


Figure 7-139. Passband Magnitude

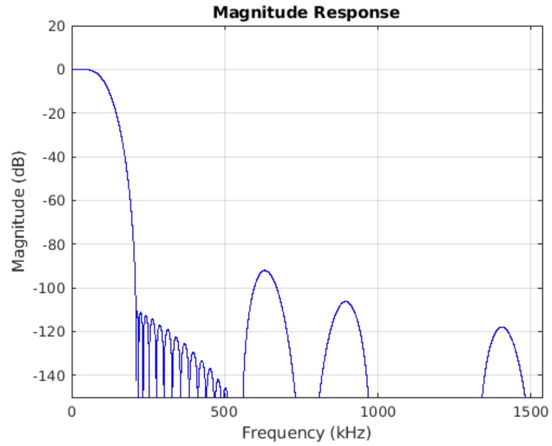


Figure 7-140. Stopband Magnitude

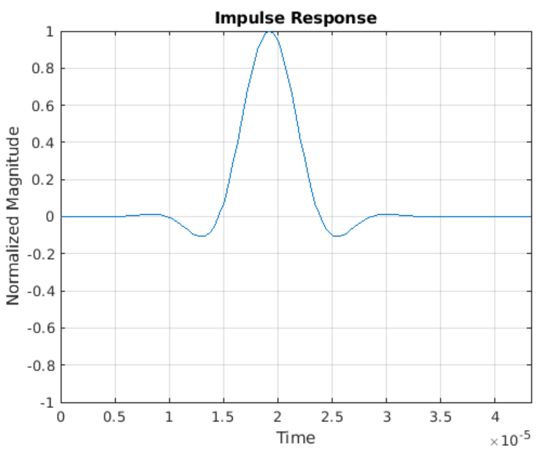


Figure 7-141. Impulse Response—Linear Phase

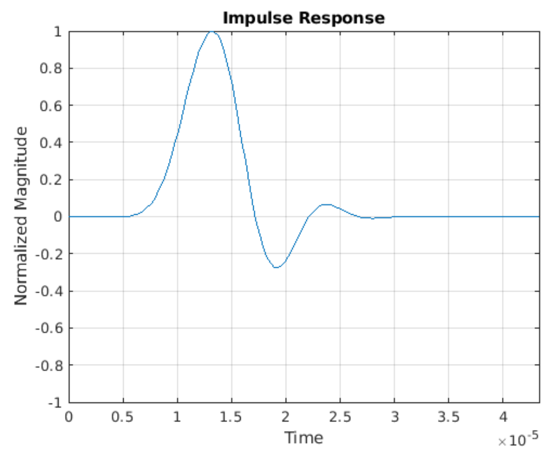


Figure 7-142. Impulse Response—Minimum Phase

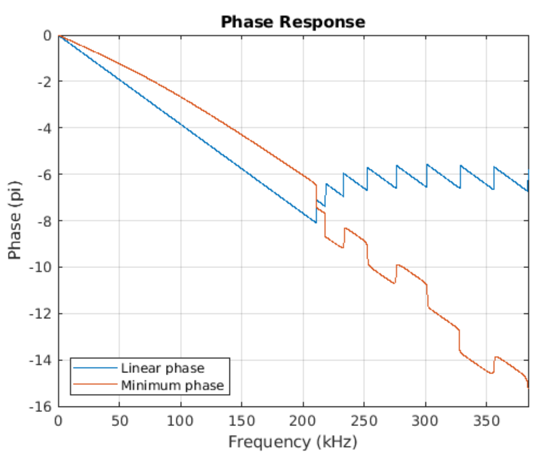


Figure 7-143. Phase vs. Frequency

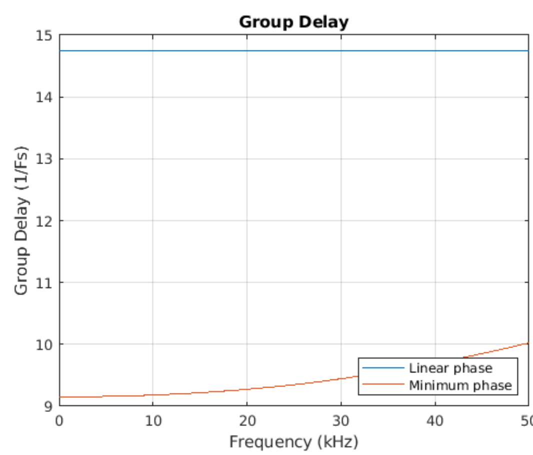


Figure 7-144. Group Delay vs. Frequency

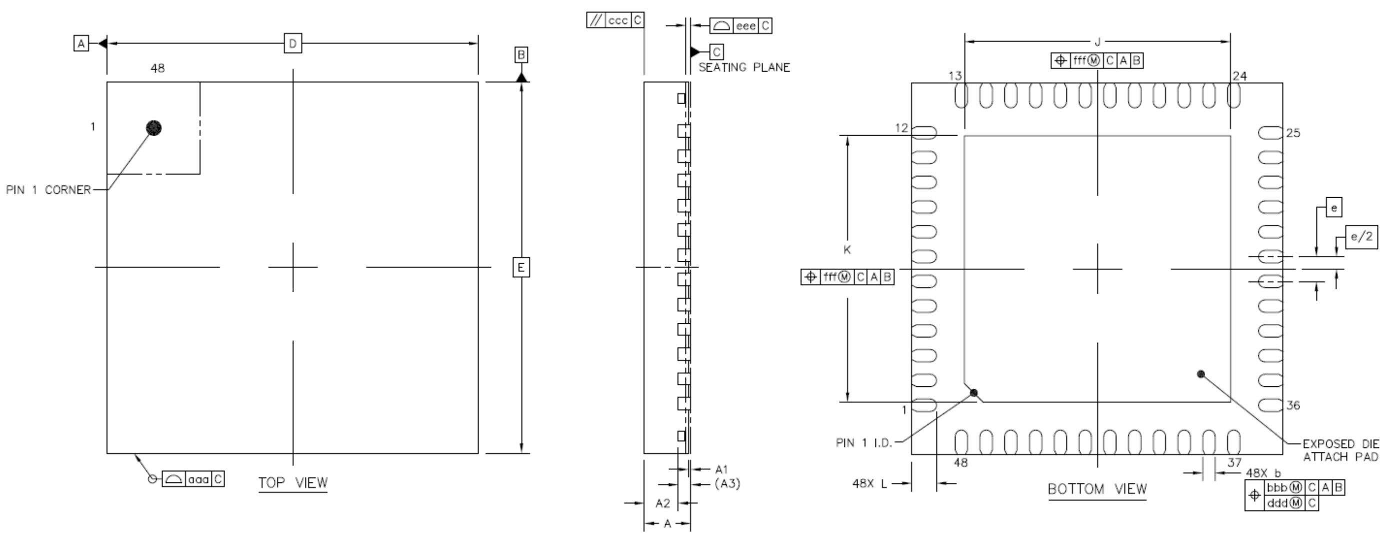
8 Thermal Characteristics

Table 8-1. Typical JEDEC Four-Layer, 2s2p Board Thermal Characteristics

Parameter	Symbol	QFN	Units
Junction-to-ambient thermal resistance	θ_{JA}	18.69	°C/W
Junction-to-board thermal resistance	θ_{JB}	5.51	°C/W
Junction-to-case (top) thermal resistance	θ_{JC}	44.75	°C/W
Junction-to-board thermal-characterization parameter	Ψ_{JB}	5.29	°C/W
Junction-to-package-top thermal-characterization parameter	Ψ_{JT}	1.26	°C/W

Notes:
- Natural convection at the maximum recommended operating temperature T_A (see Table 3-2)
- Four-layer, 2s2p PCB as specified by JESD51–9 and JESD51–11; dimensions: 101.5 x 114.5 x 1.6 mm
- Thermal parameters as defined by JESD51–12

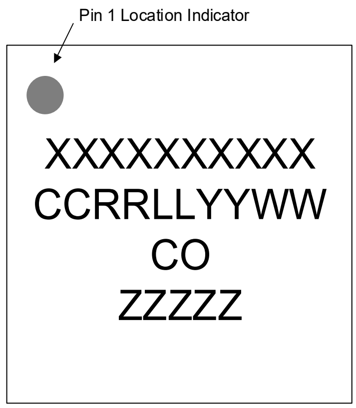
9 Package Dimensions



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203	REF
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		6	BSC
	Y	E		6	BSC
LEAD PITCH		e		0.4	BSC
EP SIZE	X	J	4.2	4.3	4.4
	Y	K	4.2	4.3	4.4
LEAD LENGTH		L	0.3	0.4	0.5
PACKAGE EDGE TOLERANCE		aaa		0.1	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
EXPOSED PAD OFFSET		fff		0.1	

Figure 9-1. QFN Package Drawing

10 Package Marking



Top Side Brand
Line 1: Part number
Line 2: Package mark
Line 3: Country of origin (CO)
Line 4: Encoded wafer/device ID

Package Mark Fields
CC = Cirrus Logic Index Code
RR = Device revision code
LL = Lot sequence code
YY = Year of manufacture
WW = Work week of manufacture

Figure 10-1. Package Marking

11 Ordering Information

Table 11-1. Ordering Information

Product	Description	Package	RoHS Compliant	Grade	Temperature Range	Container	Orderable Part Number
CS4282P	High Performance Stereo Audio Codec	48-pin QFN	Yes	Commercial	–40 to +85°C	Tray	CS4282P–DN
CS4282P	High Performance Stereo Audio Codec	48-pin QFN	Yes	Commercial	–40 to +85°C	Tape and Reel	CS4282P–DNR

12 References

- NXP Semiconductors, UM10204 Rev. 7, October 2021, *I2C-Bus Specification and User Manual*, http://www.nxp.com

13 Revision History

Table 13-1. Revision History

Revision	Changes
A1 NOV 2023	• Initial version
A2 JUN 2024	• Updated VDD_D reset thresholds (Table 3-12) • Updated “fsb” references to “fs(base)” (Section 4.2, Section 4.4.1)
A3 DEC 2024	• Recommended external components updated (Section 2) • Updated Dynamic Range and THD+N specifications (Table 3-5) • ASP_DIN setup specification updated (Table 3-14) • Thermal characteristics added (Section 8) • Orderable part numbers updated (Section 11)

Important: Please check www.cirrus.com or with your Cirrus Logic sales representative to confirm that you are using the latest revision of this document and to determine whether there are errata associated with this device.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.